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01/22/2003

Set	Items	Description
S1	8	MOSFET(W)(EDRAM OR ENHANCED(W)RAM OR ENHANCED(W)DYNAMIC(W)-RAM OR (DYNAMIC)(2N)(RANDOM(W)ACCESS(W)MEMORY) OR DRAM)
S2	0	(METAL(W)OXIDE(W)SEMICONDUCTOR(2N)TRANSISTOR)(W)(DRAM OR (-DYNAMIC(W)RANDOM(W)ACCESS(W)MEMORY))
S3	0	MOSFETS(W)(EDRAMS OR ENHANCED(W)RAMS OR ENHANCED(W)DYNAMIC-(W)RAMS OR (DYNAMIC)(2N)(RANDOM(W)ACCESS(W)MEMORIES) OR DRAMS)
S4	0	(METAL(W)OXIDE(W)SEMICONDUCTOR(2N)TRANSISTO?)(W)(DRAM? OR -(DYNAMIC(W)RANDOM(W)ACCESS(W)MEMOR?))
S5	54	(MOS OR VMOS OR NMOS OR PMOS)(W)(EDRAM? OR ENHANCED(W)RAM? OR ENHANCED(W)DYNAMIC(W)RAM? OR ((DYNAMIC)(2N)(RANDOM(W)ACCES-S(W)MEMOR?)) OR (EMBEDDED(W)DYNAMIC(W)RANDOM(W)ACCESS(W)MEMOR-?))
S6	187216	(METAL(W)OXIDE(W)SEMICONDUCTOR(2N)TRANSISTO?) OR MOS OR VM-OS OR NMOS OR PMOS OR MOSFET? ? OR CC=B2560R
S7	26813	(EDRAM? OR ENHANCED(W)RAM? OR (ENHANCED(W)DYNAMIC(W)RAM?) -OR ((DYNAMIC)(2N)(RANDOM(W)ACCESS(W)MEMOR?)) OR (RANDOM(W)ACC-ESS(W)MEMOR?))
S8	1203732	POLYSILICON OR POLY(W)(SILICON OR SI) OR SILICON OR HEXSIL OR HGH(W)600 OR KDB(W)20 OR METASILICON OR SICOMILL(W)4C OR S-ICOMILL(W)GRADE OR SILGRAIN(W)STANDARD OR SILICON(W)ELEMENT OR SILSO
S9	4	AU=(MANDELMAN JACK OR MANDELMAN, JACK OR MANDELMAN, J OR M-ANDELMAN J)
S10	20	AU=(DIVAKARUNI, RAMACHANDRA OR DIVAKARUNI RAMACHANDRA OR D-IVAKARUNI, R OR DIVAKARUNI R)
S11	4	AU=(RADENS, CARL OR RADENS CARL OR RADENS, C OR RADENS C)
S12	62	S1:S5
S13	40	RD (unique items)
S14	6	S13 AND S8
S15	0	S13 AND GATE(W)CONDUCTOR?
S16	0	S13 AND GUARD(W)RING? ?
S17	1	S13 AND (WORDLINE? ? OR WORD(W)LINE? ?)
S18	1	S13 AND (BITLINE? ? OR BIT(W)LINE? ?)
S19	3	S13 AND ARRAY
S20	0	S13 AND STRINGER?
S21	11	S14:S19
S22	29	S13 NOT S21
S23	24	S9 OR S10
S24	0	S23 AND (S1:S5)
S25	4	S23 AND S6 AND S7
S26	3	RD (unique items)
S27	2022	S6 AND S7
S28	595	S27 AND S8
S29	0	S27 AND GATE(W)CONDUCTOR?
S30	1	S27 AND GUARD(W)RING? ?
S31	85	S27 AND (WORDLINE? OR WORD(W)LINE? ?)
S32	37	S31 AND (BITLINE? OR BIT(W)LINE? ?)
S33	31	RD (unique items)
S34	31	S33 NOT S12
S35	43	S28 AND INTERCONNECT?
S36	42	S35 NOT (S12 OR S32)
S37	31	RD (unique items)

14/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

04302805 INSPEC Abstract Number: B9301-2570F-007
Title: Oxygen precipitation, internal gettering, and reliability of **silicon MOS dynamic random access memory**
Author(s): Kusakin, S.I.; Lebedev, S.V.; Litvinov, Yu.M.; Moiseenko, N.F. ; Pavlov, V.F.
Author Affiliation: F.V. Lukin Sci.-Res. Inst. of Phys. Problems, Russia
Journal: Pis'ma v Zhurnal Tekhnicheskoi Fizika vol.18, no.9-10 p. 40-2
Publication Date: May 1992 Country of Publication: Russia
CODEN: PZTFDD ISSN: 0320-0108
Translated in: Soviet Technical Physics Letters vol.18, no.5 p.291-2
Publication Date: May 1992 Country of Publication: USA
CODEN: STPLD2 ISSN: 0360-120X
U.S. Copyright Clearance Center Code: 0360-120X/92/050291-02$02.00
Language: English
Abstract: The authors consider process of internal gettering of point defects by precipitates of the type SiO/sub x/ formed in the volume of a **silicon** wafer, and the problem of incorporating internal gettering in an optimal way into a specific technological process of fabrication of MOS DRAMs. They determine the range of interstitial oxygen concentrations in the initial **silicon** wafers for which an internal getter is formed in a natural manner in the process of fabrication.
Subfile: B

14/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

01931081 INSPEC Abstract Number: B82051391, C82038756
Title: Design features and performance of a 64-kbit **MOS dynamic random access memory**
Author(s): Weidlich, R.
Author Affiliation: Werk fur Integrierte Schaltungen, Siemens AG, Munchen, West Germany
Journal: Siemens Forschungs- und Entwicklungsberichte vol.11, no.3 p.120-6
Publication Date: 1982 Country of Publication: West Germany
CODEN: SFEBBL ISSN: 0370-9736
Language: English
Abstract: The Siemens HYB 4164 device is a 64-kbit dynamic random access memory organized with 65536.1 bit and fabricated in scaled double-layer n-channel **silicon** gate technology. It is housed in a 16-pin standard dual-in-line package. Its inputs and outputs have full TTL compatibility and accept input levels between -1.5 V and +7 V. The supply voltage is 5 V (+or-10%); the negative substrate bias voltage required for operation is supplied by an on-chip bias generator. The external refresh requirement is 256 refresh cycles every 4 ms. All chips are coated with polyimide for protection against alpha radiation.
Subfile: B C

14/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

01413277 INSPEC Abstract Number: B79042632, C79030059
Title: A 64 Kbit **MOS dynamic random access memory**
Author(s): Natori, K.; Ogura, M.; Maeguchi, K.; Taguchi, S.; Iwai, H.
Author Affiliation: Toshiba Res. & Dev. Center, Toshiba Corp., Kawasaki, Japan
Journal: IEEE Journal of Solid-State Circuits vol.SC-14, no.2 p. 482-5
Publication Date: April 1979 Country of Publication: USA
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: A 65536 word*1 bit dynamic random access memory is developed using 4 mu m design rules, a 320-AA thick gate oxide film, and an improved double-poly n-channel **silicon** gate process. The chip is successfully encapsulated in a standard 16-pin dual-in-line ceramic package, and is able to take over the place that the current 16 Kbit dynamic RAM has occupied. It realizes high speed operation with access time of less than 100 ns and low power dissipation of less than 300 mW.
Subfile: B C

14/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

00988193 INSPEC Abstract Number: B76046418, C76031609
Title: A high-speed 16-kbit n-MOS random-access memory
Author(s): Itoh, K.; Shimohigashi, K.; Chiba, K.; Taniguchi, K.; Kawamoto, H.
Author Affiliation: Central Res. Lab., Hitachi Ltd., Tokyo, Japan
Journal: IEEE Journal of Solid-State Circuits vol.SC-11, no.5 p. 585-90
Publication Date: Oct. 1976 Country of Publication: USA
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: This paper presents one version of a high-speed 16-kbit **dynamic MOS random-access memory** (RAM). This memory utilizes a one transistor cell with an area of 22*36 mu m/sup 2/ which is fabricated using advanced n-channel **silicon** -gate MOS technology (5- mu m photolithography). The main feature of the design is a sense circuitry scheme, which allows a high speed (read access time of 200 ns) with low-power dissipation (600 mW at the 400-ns cycle time). The fully decoded memory is fabricated on a 5*7 mm/sup 2/ chip and is assembled in a 22-lead ceramic dual-in-line package.
Subfile: B C

14/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

00564570 INSPEC Abstract Number: B73035352, C73022815
Title: A 4K **MOS dynamic random-access memory**
Author(s): Abbott, R.A.; Regitz, W.M.; Karp, J.A.
Author Affiliation: INTEL Corp., Santa Clara, CA, USA
Journal: IEEE Journal of Solid-State Circuits vol.SC-8, no.5 p. 292-8
Publication Date: Oct. 1973 Country of Publication: USA
CODEN: IJSCBC ISSN: 0018-9200
Language: English

01/22/2003

Abstract: Presents one version of a 4K **dynamic MOS random-access memory** utilizing a 3 device/bit cell with an area of less than 2 mil/sup 2//b, which is fabricated using an n-channel **silicon** gate MOS technology. The chip requires only a single phase clock and internally generates the multiphase timing required. Other than the single high voltage clock, all inputs and the output are TTL compatible.
Subfile: B C

14/3,AB/6 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03432709
E.I. Monthly No: EIM9205-027295
Title: Unified generation model with donor and acceptor-type trap states for heavily doped **silicon**.
Author: Voldman, Steven H.; Johnson, Jeffrey B.; Linton, Thomas D.; Titcomb, Stephen L.
Corporate Source: IBM, Essex Junction, VT, USA
Conference Title: 1990 International Electron Devices Meeting
Conference Location: San Francisco, CA, USA Conference Date: 19901209
E.I. Conference No.: 16230
Source: Technical Digest - International Electron Devices Meeting. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 90CH2865-4). p 349-352
Publication Year: 1990
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: A quasi-classical generation formulation is analytically developed for heavily doped **silicon** where electric field phenomena are important. This quasi-classical formalism is suitable for modeling thermal and electric field-dependent leakage mechanisms in semiconductor structures with multiple trap state types and populations. The formalism is valuable in the explanation of the heavily-doped gate-diode leakage characteristic in 4- to 64-Mb p** plus substrate-plate-trench DRAM cells and p-channel MOSFETs. The development is implemented into a three-dimensional (3-D) finite-element device simulator (FIELDAY II), advancing VLSI device modeling. 11 Refs.

21/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

04302805 INSPEC Abstract Number: B9301-2570F-007
Title: Oxygen precipitation, internal gettering, and reliability of **silicon MOS dynamic random access memory**
Author(s): Kusakin, S.I.; Lebedev, S.V.; Litvinov, Yu.M.; Moiseenko, N.F.; Pavlov, V.F.
Author Affiliation: F.V. Lukin Sci.-Res. Inst. of Phys. Problems, Russia
Journal: Pis'ma v Zhurnal Tekhnicheskoi Fizika vol.18, no.9-10 p. 40-2
Publication Date: May 1992 Country of Publication: Russia
CODEN: PZTFDD ISSN: 0320-0108
Translated in: Soviet Technical Physics Letters vol.18, no.5 p.291-2
Publication Date: May 1992 Country of Publication: USA
CODEN: STPLD2 ISSN: 0360-120X
U.S. Copyright Clearance Center Code: 0360-120X/92/050291-02$02.00
Language: English
Abstract: The authors consider process of internal gettering of point defects by precipitates of the type SiO/sub x/ formed in the volume of a **silicon** wafer, and the problem of incorporating internal gettering in an optimal way into a specific technological process of fabrication of MOS DRAMs. They determine the range of interstitial oxygen concentrations in the initial **silicon** wafers for which an internal getter is formed in a natural manner in the process of fabrication.
Subfile: B

21/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

03960299 INSPEC Abstract Number: B91055169, C91058050
Title: Recent DRAM technology
Author(s): Iijima, H.; Hori, R.; Ishihara, M.
Author Affiliation: Hitachi Ltd., Tokyo, Japan
Journal: Hitachi Review vol.40, no.1 p.7-16
Publication Date: Feb. 1991 Country of Publication: Japan
CODEN: HITAAQ ISSN: 0018-277X
Language: English
Abstract: High speed and high density metal oxide semiconductor (**MOS**) **dynamic random access memory** (DRAM) have been required according to the high performance of microprocessor apparatus. A 4 Mbit DRAM and a 1 Mbit BiCMOS DRAM have been realized by employing 0.8 mu m CMOS and 1.3 mu m BiCMOS technology by developing high speed and low power dissipation circuits. High speed and high reliability have been realized in the 4 Mbit DRAM by adopting a transposed **bit line** structure, the multiple layer wiring technique, and the stacked capacitor memory cell structure. The 35 ns access time of the 1 Mbit BiCMOS DRAM, the fastest in the world, has been realized by integrating BiCMOS circuits.
Subfile: B C

21/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

01/22/2003

03395943 INSPEC Abstract Number: B89042153, C89038308
Title: A fault model for multivalued **NMOS dynamic random access memories**
Author(s): Venkatapathi Naidu, R.; Mahapatra, S.
Author Affiliation: Adv. Centre for Res. in Electron., Indian Inst. of Technol., Bombay, India
Journal: Microelectronics and Reliability vol.29, no.2 p.137-43
Publication Date: 1989 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
U.S. Copyright Clearance Center Code: 0026-2714/89/$3.00+.00
Language: English
Abstract: A multivalued **NMOS dynamic random access memory** configuration is proposed. A basic NMOS dynamic RAM cell with multivalued logic operation is discussed. An 8-state multivalued NMOS dynamic RAM configuration is developed. The working principle of 8-state multivalued NMOS dynamic RAM with WRITE/READ mode of operation is discussed. A fault model for multivalued NMOS dynamic RAM is proposed. Various functional failures occurring in multivalued NMOS dynamic RAMs are highlighted. A computational procedure is given for computing the probabilities of various failure distributions in the memory cell **array** rows for a given number of failed memory cells. Combined with the proposed failure model for the individual memory cells, the results can be used to compute probabilities about the performance of the memory cell **array**.
Subfile: B C

21/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

01999762 INSPEC Abstract Number: B83012163, C83009421
Title: A 64K-MOS-DRAM: reliability and performance
Author(s): Weidlich, R.
Author Affiliation: Component Div., Siemens AG, Munich, West Germany
Conference Title: Reliability in Electrical and Electronic Components and Systems. Fifth European Conference on Electrotechnics - EUROCON '82 p. 275-7
Editor(s): Lauger, E.; Moltoft, J.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1982 Country of Publication: Netherlands xxxvii+1171 pp.
ISBN: 0 444 86419 9
Conference Sponsor: IEEE; Convention Nat. Soc. Electr. Eng. Western Europe
Conference Date: 14-18 June 1982 Conference Location: Copenhagen, Denmark
Language: English
Abstract: A single 5 V supply, 64K-bit **dynamic MOS random access memory** using a high cell charge, boostet **word-lines**, quiet **word-line** flip-flops, and some other new design features has been developed and is fabricated with a high reliable scaled n-channel double Si gate technology. TTL compatible with multiplexed address inputs and is housed in a standard 16 pin side-brazed ceramic or plastic package.
Subfile: B C

21/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

01931081 INSPEC Abstract Number: B82051391, C82038756
Title: Design features and performance of a 64-kbit **MOS dynamic random access memory**
Author(s): Weidlich, R.
Author Affiliation: Werk fur Integrierte Schaltungen, Siemens AG, Munchen, West Germany
Journal: Siemens Forschungs- und Entwicklungsberichte vol.11, no.3 p.120-6
Publication Date: 1982 Country of Publication: West Germany
CODEN: SFEBBL ISSN: 0370-9736
Language: English
Abstract: The Siemens HYB 4164 device is a 64-kbit dynamic random access memory organized with 65536.1 bit and fabricated in scaled double-layer n-channel **silicon** gate technology. It is housed in a 16-pin standard dual-in-line package. Its inputs and outputs have full TTL compatibility and accept input levels between -1.5 V and +7 V. The supply voltage is 5 V (+or-10%); the negative substrate bias voltage required for operation is supplied by an on-chip bias generator. The external refresh requirement is 256 refresh cycles every 4 ms. All chips are coated with polyimide for protection against alpha radiation.
Subfile: B C

21/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

01413277 INSPEC Abstract Number: B79042632, C79030059
Title: A 64 Kbit **MOS dynamic random access memory**
Author(s): Natori, K.; Ogura, M.; Maeguchi, K.; Taguchi, S.; Iwai, H.
Author Affiliation: Toshiba Res. & Dev. Center, Toshiba Corp., Kawasaki, Japan
Journal: IEEE Journal of Solid-State Circuits vol.SC-14, no.2 p. 482-5
Publication Date: April 1979 Country of Publication: USA
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: A 65536 word*1 bit dynamic random access memory is developed using 4 mu m design rules, a 320-AA thick gate oxide film, and an improved double-poly n-channel **silicon** gate process. The chip is successfully encapsulated in a standard 16-pin dual-in-line ceramic package, and is able to take over the place that the current 16 Kbit dynamic RAM has occupied. It realizes high speed operation with access time of less than 100 ns and low power dissipation of less than 300 mW.
Subfile: B C

21/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

00988193 INSPEC Abstract Number: B76046418, C76031609
Title: A high-speed 16-kbit n-MOS random-access memory
Author(s): Itoh, K.; Shimohigashi, K.; Chiba, K.; Taniguchi, K.; Kawamoto, H.
Author Affiliation: Central Res. Lab., Hitachi Ltd., Tokyo, Japan
Journal: IEEE Journal of Solid-State Circuits vol.SC-11, no.5 p. 585-90
Publication Date: Oct. 1976 Country of Publication: USA

CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: This paper presents one version of a high-speed 16-kbit **dynamic MOS random-access memory** (RAM). This memory utilizes a one transistor cell with an area of 22*36 mu m/sup 2/ which is fabricated using advanced n-channel **silicon** -gate MOS technology (5- mu m photolithography). The main feature of the design is a sense circuitry scheme, which allows a high speed (read access time of 200 ns) with low-power dissipation (600 mW at the 400-ns cycle time). The fully decoded memory is fabricated on a 5*7 mm/sup 2/ chip and is assembled in a 22-lead ceramic dual-in-line package.
Subfile: B C

21/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

00564570 INSPEC Abstract Number: B73035352, C73022815
Title: A 4K **MOS dynamic random-access memory**
Author(s): Abbott, R.A.; Regitz, W.M.; Karp, J.A.
Author Affiliation: INTEL Corp., Santa Clara, CA, USA
Journal: IEEE Journal of Solid-State Circuits vol.SC-8, no.5 p. 292-8
Publication Date: Oct. 1973 Country of Publication: USA
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: Presents one version of a 4K **dynamic MOS random-access memory** utilizing a 3 device/bit cell with an area of less than 2 mil/sup 2//b, which is fabricated using an n-channel **silicon** gate MOS technology. The chip requires only a single phase clock and internally generates the multiphase timing required. Other than the single high voltage clock, all inputs and the output are TTL compatible.
Subfile: B C

21/3,AB/9 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03432709
E.I. Monthly No: EIM9205-027295
Title: Unified generation model with donor and acceptor-type trap states for heavily doped **silicon**.
Author: Voldman, Steven H.; Johnson, Jeffrey B.; Linton, Thomas D.; Titcomb, Stephen L.
Corporate Source: IBM, Essex Junction, VT, USA
Conference Title: 1990 International Electron Devices Meeting
Conference Location: San Francisco, CA, USA Conference Date: 19901209
E.I. Conference No.: 16230
Source: Technical Digest - International Electron Devices Meeting. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 90CH2865-4). p 349-352
Publication Year: 1990
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: A quasi-classical generation formulation is analytically developed for heavily doped **silicon** where electric field phenomena are important. This quasi-classical formalism is suitable for modeling thermal and electric field-dependent leakage mechanisms in semiconductor

structures with multiple trap state types and populations. The formalism is valuable in the explanation of the heavily-doped gate-diode leakage characteristic in 4- to 64-Mb p** plus substrate-plate-trench DRAM cells and p-channel MOSFETs. The development is implemented into a three-dimensional (3-D) finite-element device simulator (FIELDAY II), advancing VLSI device modeling. 11 Refs.

21/3,AB/10 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02798160
E.I. Monthly No: EI8910100479
Title: Fault model for multivalued **NMOS dynamic random access memories**.
Author: Venkatapathi, R.; Mahapatra, S.
Corporate Source: Indian Inst of Technology, Bombay, India
Source: Microelectronics and Reliability v 29 n 2 1989 p 137-143
Publication Year: 1989
CODEN: MCRLAS ISSN: 0026-2714
Language: English
Abstract: A multivalued **NMOS dynamic random access memory** configuration is proposed. A basic NMOS dynamic RAM cell with multivalued logic operation is discussed. An 8-state multivalued NMOS dynamic RAM configuration is developed. The working principle of 8-state multivalued NMOS dynamic RAM with WRITE/READ mode of operation is discussed. A fault model for multivalued NMOS dynamic RAM is proposed. Various functional failures occurring in multivalued NMOS dynamic RAMs are highlighted. A computational procedure is given for computing the probabilities of various failure distributions in the memory cell **array** rows for a given number of failed memory cells. Combined with the proposed failure model for the individual memory cells, the results can be used to compute probabilities about the performance of the memory cell **array**. (Author abstract) 3 Refs.

21/3,AB/11 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01941238
E.I. Monthly No: EI8602010721
E.I. Yearly No: EI86031171
Title: CORRUGATED CAPACITOR CELL (CCC).
Author: Sunami, Hideo; Kure, Tokuo; Hashimoto, Norikazu; Itoh, Kiyoo; Toyabe, Toru; Asai, Shojiro
Corporate Source: Hitachi Ltd, Fundamental Si Process Development Group, Kokubunji, Jpn
Source: IEEE Transactions on Electron Devices v ED-31 n 6 Jun 1984 p 746-753
Publication Year: 1984
CODEN: IETDAI ISSN: 0018-9383
Language: ENGLISH
Abstract: A new **MOS dynamic random access memory** (dRAM) cell named 'CCC' has been successfully developed based on a one-device cell concept. This CCC is characterized by an etched-moat storage-capacitor extended into the substrate, resulting in almost independent increase in storage capacitance C//S of its cell size. A typical C//S value of 60 fF has been obtained with 3 X 7 MU m**2 CCC having a 4- MU m deep moat and a capacitor insulator equivalent to 15 nm SiO//2 in

thickness. The CCC is discussed in terms of its capacitance characteristics, dRAM operation with unit 32-Kbit **array**, some limiting factor to its closer packing, and future considerations. (Author abstract) 11 refs.
?

22/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

04145193 INSPEC Abstract Number: A9212-7755-001, B9206-2810F-002
Title: Polarization reversal and high dielectric permittivity in lead magnesium niobate titanate thin films
Author(s): Udayakumar, K.R.; Chen, J.; Schuele, P.J.; Cross, L.E.; Kumar, V.; Krupanidhi, S.B.
Author Affiliation: Mater. Res. Lab., Pennsylvania State Univ., University Park, PA, USA
Journal: Applied Physics Letters vol.60, no.10 p.1187-9
Publication Date: 9 March 1992 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
U.S. Copyright Clearance Center Code: 0003-6951/92/101187-03$03.00
Language: English
Abstract: Ferroelectric thin films of the morphotropic phase boundary composition in the lead magnesium niobate-lead titanate solid solution system were fabricated through the sol-gel spin-on technique. The rapid thermally annealed films showed a very high dielectric constant of 2900, with a concomitant low dissipation factor of 0.02; the films were hysteretic with a saturation remanence of 11 mu C/cm/sup 2/ and a coercive voltage of 0.5 V. The storage charge density observed at 5 V was 210 fC/ mu m/sup 2/ . These films merit consideration for potential application in ferroelectric nonvolatile random access memories (NVRAMs), and in high bit density metal-oxide-semiconductor (**MOS**) **dynamic random access memories** (DRAMs).
Subfile: A B

22/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

03335242 INSPEC Abstract Number: B89022720
Title: Power reduction methods for **NMOS dynamic random access memories**
Author(s): Naidu, R.V.; Mahapatra, S.
Author Affiliation: Adv. Centre for Res. in Electron., Indian Inst. of Technol., Bombay, India
Journal: Microelectronics and Reliability vol.28, no.6 p.877-83
Publication Date: 1988 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
U.S. Copyright Clearance Center Code: 0026-2714/88/$3.00+.00
Language: English
Abstract: Power reduction methods for **NMOS dynamic random access memories** are proposed which reduce power dissipation. As the bit density increases in **NMOS dynamic random access memories** the power dissipation increases. A major consideration in the design of megabit dynamic random access memories is the power supply voltage. The power supply voltage mainly depends upon the following factors: power dissipation; reliability, such as high field effects due to small device size; memory cell operating margin. Power dissipation in decoders and 1 megabit **NMOS dynamic random access memory** chips are discussed. The basic properties of the proposed methods and a prototype VLSI implementation are discussed. In order to meet user power supply requirements, the proposed power reduction methods are useful for future megabit **NMOS dynamic random access memories**.
Subfile: B

22/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

03220633 INSPEC Abstract Number: C88057516
Title: Inflate your Atari
Author(s): Leray, J.; Quero, J.-C.; Pommier, B.
Journal: Micro Systemes no.88 p.147-55
Publication Date: July-Aug. 1988 Country of Publication: France
CODEN: MSYSDT ISSN: 0183-5084
Language: French
Abstract: Instructions are given for enhancing the power of an ST series microcomputer with personalised extension cards giving access to about 11.5 M of extra memory. A block diagram and layouts of the linking card are accompanied by a memory map, and pin diagrams of the PAL circuits. Appendices cover these circuits as well as the external and internal configurations of the 68000 chip and **MOS dynamic random-access memories**.
Subfile: C

22/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

03155013 INSPEC Abstract Number: B88038521, C88034859
Title: Fault tolerance in N-**MOS random access memories** with **dynamic** redundancy methods
Author(s): Naidu, R.V.; Mahapatra, S.
Author Affiliation: Adv. Centre for Res. in Electron., Indian Inst. of Technol., Bombay, India
Journal: Microelectronics and Reliability vol.28, no.2 p.193-200
Publication Date: 1988 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
U.S. Copyright Clearance Center Code: 0026-2714/88/$3.00+.00
Language: English
Abstract: Two methods of dynamic redundancy are discussed which allow the treatment of memory chip faults at the interface of the main memory. The first approach is a standby system where the I/O lines of the memory can be dynamically switched to spare bit slices. This task is performed by a switching network implemented at the memory interface. Every memory access is controlled by a fault status table (FST) which memorizes the fault conditions of each memory block. This fault status table is also implemented outside the memory system. The basic properties of the proposed methods and a prototype VLSI implementation are discussed. Then a corresponding method for memory reconfiguration by means of graceful degradation is discussed. The memory reliabilities implied by both the methods are estimated. These two methods have considerable importance in reliability when compared to conventional methods. The major advantage is that the size of reconfiguration of the system can be considerably reduced.
Subfile: B C

22/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

02860511 INSPEC Abstract Number: B87024169, C87022570
Title: Alpha particle induced soft errors in NMOS RAMs: a review

Author(s): Carter, P.M.; Wilkins, B.R.
Author Affiliation: Dept. of Electron. & Comput. Sci., Southampton Univ., UK
Journal: IEE Proceedings I (Solid-State and Electron Devices) vol.134, no.1 p.32-44
Publication Date: Feb. 1987 Country of Publication: UK
CODEN: IPIDD9 ISSN: 0143-7100
U.S. Copyright Clearance Center Code: 0143-7100/87/$2.00+0.00
Language: English
Abstract: The authors aim to explain the alpha particle induced soft error phenomenon using the **NMOS dynamic random access memory** (RAM) as a model. They discuss some of the many techniques experimented with by manufacturers to overcome the problem, and give a review of the literature covering most aspects of soft errors in dynamic RAMs. Finally, the soft error performance of current dynamic RAM and static RAM products from several manufacturers are compared.
Subfile: B C

22/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

02713768 INSPEC Abstract Number: B86046852
Title: Cell structures for future DRAMs
Author(s): Sunami, H.
Author Affiliation: Hitachi Ltd., Tokyo, Japan
Conference Title: International Electron Devices Meeting. Technical Digest (Cat. No. 85CH2252-5) p.694-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1985 Country of Publication: USA 772 pp.
U.S. Copyright Clearance Center Code: CH2252-5/85/0000-0694$01.00
Conference Sponsor: IEEE
Conference Date: 1-4 Dec. 1985 Conference Location: Washington, DC, USA
Language: English
Abstract: The trends in **MOS dynamic random-access memories** (DRAMs) are reviewed with emphasis on the memory cell structures. A projected trend in the scalability of future DRAMs is discussed on the basis of this review. Another concern is how far beyond 1 Mb the one-device cell will go. With vertically stacked cells, the one-device cell can reach the ultimately simple configuration, i.e. only one transistor in the horizontal cell region. Thus, no alternative superior to the one-device cell is found in this review. Finally, some candidates which are assumed to be suitable for memory cells of future DRAMs are proposed.
Subfile: B

22/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

02636475 INSPEC Abstract Number: B86020552, C86018378
Title: Trends in megabit DRAMs
Author(s): Sunami, H.; Asai, S.
Author Affiliation: Central Res. Lab., Hitachi Ltd., Kokubunji, Tokyo, Japan
Conference Title: 1985 International Symposium on VLSI Technology, Systems and Applications. Proceedings of Technical Papers p.4-8
Publisher: ERSO, Hsinchu, Taiwan

Publication Date: 1985 Country of Publication: Taiwan 355 pp.
Conference Sponsor: Nat. Sci. Council; Ind. Technol. Res. Inst
Conference Date: 8-10 May 1985 Conference Location: Taipei, Taiwan
Language: English
Abstract: The past and the future trends in **MOS dynamic random-access memories** (DRAMs) are reviewed in terms of the memory cells, DRAM functions, and fabrication technologies. On the basis of the review, projected trends in coming megabit DRAMs are forecasted.
Subfile: B C

22/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

01409361 INSPEC Abstract Number: B79042657, C79027177
Title: Reliability of **dynamic MOS random access memories**. II
Author(s): Bajenesco, T.I.
Journal: Revue Polytechnique no.12 p.1425, 1427, 1429
Publication Date: 25 Dec. 1978 Country of Publication: Switzerland
CODEN: RVPTBR ISSN: 0374-4256
Language: French
Abstract: For pt.I see ibid., no.1379, p.1297, 1299, 1301, 1303 (Nov. 1978). The mean time between failures is considered as a function of the number of modules in the memory, and the cause of errors is discussed. Test methods are described and circuit precautions to minimise failure are suggested.
Subfile: B C

22/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

00773112 INSPEC Abstract Number: B75019228, C75015073
Title: Shift register generates system timing
Author(s): Cook, H.
Author Affiliation: Texas Instruments Ltd., Bedford, UK
Journal: Electronic Engineering vol.47, no.566 p.23, 25
Publication Date: April 1975 Country of Publication: UK
CODEN: ELCEA9 ISSN: 0013-4902
Language: English
Abstract: The design of electronic systems requires the internal generation of a control clock waveform. An example of this is in the memories using **dynamic mos random access memory** devices. A very simple method is to use a parallel-loading shift register. To illustrate the principle, a clock waveform generator suitable for use with the Texas Instruments TMS4030-a 4096-bit ram-is described. This device requires a chip-enable clock pulse of 320 ns minimum and a minimum cycle time of 470 ns. The accuracy with which this may be generated is a function of the number of shift register stages employed.
Subfile: B C

22/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

00467200 INSPEC Abstract Number: C73002765

01/22/2003

Title: TV set is display for data terminal
Author(s): Bratt, B.
Author Affiliation: Motorola Inc., Phoenix. AZ, USA
Journal: Electronic Design vol.20, no.19 p.134-41
Publication Date: 14 Sept. 1972 Country of Publication: USA
CODEN: ELODAW ISSN: 0013-4872
Language: English
Abstract: The article describes an all-digital character- generation system using a TV receiver for data display. Using dynamic M.O.S. random access memories, the system has a capacity of 1024 characters, each generated by a 5*7 dot matrix. A full set of 64 ASCII alphanumeric characters is available.
Subfile: C

22/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

00265018 INSPEC Abstract Number: C71012748
Title: Semiconductor memory system design
Author(s): lund, T.
Conference Title: Man made memories, conference summaries p.1 pp.
Publisher: Business Conferences and Exhibitions, London, UK
Publication Date: 1971 Country of Publication: UK 19 pp.
Conference Sponsor: Electron. Equipment News; Microelectronics
Conference Date: 30-31 March 1971 Conference Location: London, UK
Language: English
Abstract: This paper describes in detail two semiconductor memory systems, both realized with 1024 bit **dynamic MOS random access memory** chips. These two systems represent two ways to organise the peripheral circuits for this type of memory component. The data output is presented at strobe time to a common data bus on the backplane. The controller and level shift circuits (TTL to MOS) are located on separated boards, hence making the memory system easily expandable. The major problem the user is likely to encounter with dynamic MOS circuits used with TTL logic, is noise due to high capacitive charging currents. This paper describes in detail how such noise problems may be averted. The problem of volatility in semiconductor memories is described in detail and a section is included on backup power systems. There is also a description on how to minimize the power consumption during low power standby operation. Detailed performance specifications are included.
Subfile: C

22/3,AB/12 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1549563 NTIS Accession Number: PB91-124867
National Technical Report (Matsushita Electric Industrial Company), Vol. 36, No. 4, August 1990. Special Issue: Semiconductors (2)
Matsushita Electric Industrial Co. Ltd., Moriguchi (Japan).
Corp. Source Codes: 088966000
c1990 145p
Languages: Japanese
Journal Announcement: GRAI9105
Text in Japanese with English abstracts. See also PB91-124875 through PB91-124941 and PB91-124842. Portions of this document are not fully legible.
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customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A07/MF A01
Contents: 10-bit Bi-CMOS A/D Converter AN8130K for Hi-Vision; Single Chip Luminance and Chrominance Signal Processing IC AN3450 for VTRs; Cathode Driver IC for PDP DN8874SB/SBR; Super Low-Noise HEMT 2SK1687/1688; GaAs Power Amplifier Module for Portable Telephones; AlGaAs/GaAs Heterojunction Bipolar Transistors for High Speed and High Frequency Devices; Electron-Beam Writing Technology in Semiconductor Fabrication; Proximity Effect Correction System for Electron Beam Direct Writing; High Transparency Resist for KrF Excimer Laser Lithography; Holographic Nanometer Alignment for Wafer Stepper; Photolithography Using VUV Light Source--Nanometer Pattern Transfer--; 1/4 micrometer Large-Tilt-Angle Implanted Drain (LATID) Device Technology; Very High Speed Bipolar Integrated Circuit Process Using Self-Aligned Technology; Evaluation Technology of VLSI Reliability Using Hot Carrier Luminescence; Reliability on Soldering Heat Stress of SMDs; Reliability Evaluation Using TEG on Fine Pattern Process of Semiconductors; Reliability of 4M-bit DRAM MN41C4000 Series.

22/3,AB/13 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02922338
E.I. Monthly No: EI9007085278
Title: Alpha-particle induced source-drain penetration (ALPEN) effects.
Author: Hisamoto, Digh; Toyabe, Tohru; Takeda, Eiji
Corporate Source: Hitachi Ltd, Hitachi, Jpn
Source: Electronics & Communications in Japan. Part II: Electronics v 72 n 8 Aug 1989 p 96-102
Publication Year: 1989
CODEN: ECJEEJ ISSN: 8756-663X
Language: English
Abstract: The source-drain penetration (ALPEN) effect, which is a new alpha -particle induced soft error mechanism, was found and investigated by using a 3-dimensional simulation. This error mechanism was also confirmed experimentally. The influence of this effect on future devices is predicted, and it has been shown that a device with a channel length shorter than 0.5 mu m is influenced strongly by this effect. Therefore, it was concluded that this effect is an important factor in the scaling limit of a device. (Edited author abstract) 12 Refs.

22/3,AB/14 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02729230
E.I. Monthly No: EI8904038009
Title: Design methodology and size limitations of submicrometer MOSFET's for DRAM application.
Author: Lee, Win-How; Osakama, Todomu; Asada, Kunihiro; Sugano, Takuo
Corporate Source: Univ of Tokyo, Tokyo, Jpn
Source: IEEE Transactions on Electron Devices v 35 n 11 Nov 1988 p 1876-1884
Publication Year: 1988
CODEN: IETDAI ISSN: 0018-9383
Language: English

Abstract: A design methodology of submicrometer MOSFETs for a one-transistor DRAM (dynamic random-access memory) cell is proposed. The methodology takes into account physical limiting phenomena such as (1) avalanche breakdown at the drain junction; (2) bulk punchthrough; (3) short-channel effect, and (4) hot-electron effect, and circuit-performance requirements such as (5) leakage current; (6) access delay; (7) noise margin, and (8) alpha -particle-induced soft error. A minimum metallurgical channel length is 0.42 mu m at a circuit voltage of 2.8 V for a planar cell structure. Although these parameters are derived assuming a planar cell, the design method can be applied to advanced cell structures, such as stacked and trench cell structures, by setting adjustable design parameters for the area and capacitor factors of a memory cell. 40 Refs.

22/3,AB/15 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02622170
E.I. Monthly No: EI8808072127
Title: FAULT TOLERANCE IN N-**MOS** **RANDOM** **ACCESS** **MEMORIES** WITH **DYNAMIC** REDUNDANCY METHODS.
Author: Venkatapathi Naidu, R.; Mahapatra, S.
Corporate Source: Indian Inst of Technology, Bombay, India
Source: Microelectronics and Reliability v 28 n 2 1988 p 193-200
Publication Year: 1988
CODEN: MCRLAS ISSN: 0026-2714
Language: English
Abstract: Two methods of dynamic redundancy are discussed which allow the treatment of memory chip faults at the interface of the main memory. The first approach is a standby system where the I/O lines of the memory can be dynamically switched to spare bit slices. This task is performed by a switching network implemented at the memory interface. Every memory access is controlled by a fault status table (FST) which memorizes the fault conditions of each memory block. This fault status table is also implemented outside the memory system. The basic properties of the proposed methods and a prototype VLSI implementation are discussed. A corresponding method for memory reconfiguration by means of graceful degradation is discussed. The memory reliabilities implied by both methods are estimated. These two methods are important in reliability when compared to conventional methods. The major advantage is that the size of reconfiguration of the system can be considerably reduced. (Edited author abstract) 10 refs.

22/3,AB/16 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02258467
E.I. Monthly No: EIM8707-044859
Title: TRENCH TRANSISTOR CELL WITH SELF-ALIGNED CONTACT (TSAC) FOR MEGABIT MOS DRAM.
Author: Yanagisawa, Masayuki; Nakamura, Kunio; Kikuchi, Masanori
Corporate Source: NEC, Sagamihara, Jpn
Conference Title: International Electron Devices Meeting 1986: IEDM - Technical Digest. International Electron Devices Meeting 1986: IEDM - Technical Digest.
Conference Location: Los Angeles, CA, USA Conference Date: 19861207
E.I. Conference No.: 09693
Source: Technical Digest - International Electron Devices Meeting 1986.

Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (Cat n 86CH2381-2), Piscataway, NJ, USA p 132-135
Publication Year: 1986
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: A one-transistor, one-capacitor MOS dynamic RAM (DRAM) cell structure called the trench transistor cell with self-aligned contact (TSAC) has been developed. The feature of this RAM cell is shrinkage of the conventional trench capacitor cell by combination of the trench transistor and the self-aligned contact. With submicron design rule, cell size can be reduced to below 9 MU m**2 and the TSAC is suitable for construction of a reasonable size 4 Mb DRAM. 9 refs.

22/3,AB/17 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01551955
E.I. Monthly No: EI8408076072
E.I. Yearly No: EI84031909
Title: C-MOS 256-K RAM WITH WIDEBAND OUTPUT STANDS BY ON MICROWATTS.
Author: Mohsen, Amr; Kung, Roger; Schutz, Joe; Madland, Paul; Simonsen, Carl; Hamdy, Esmat; Yu, Ken
Corporate Source: Intel Corp, Portland, Oreg, USA
Source: Electronics v 57 n 12 Jun 14 1984 p 138-143
Publication Year: 1984
CODEN: ELECAD ISSN: 0013-5070
Language: ENGLISH
Abstract: A 256-K-by-1-bit dynamic random-access memory developed with a high-performance complementary-MOS (C-MOS) technology is presented as an example of using C-MOS to provide effective solutions to critical device and circuit problems in dynamic-RAM design. The use of a novel architecture and innovative circuits to offer features not previously implemented in n-channel MOS designs is illustrated. The device offers high-speed row access and high column-data bandwidth to meet the requirements of high-performance cache-memory systems, bit-mapped graphics displays, and signal processing.

22/3,AB/18 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01082782
E.I. Monthly No: EI8112098430
E.I. Yearly No: EI81024599
Title: MEMORIES.
Author: Posa, John G.
Source: Electronics v 53 n 23 Oct 23 1980 p 132-136, 141-142, 145
Publication Year: 1980
CODEN: ELECAD ISSN: 0013-5070
Language: ENGLISH
Abstract: In spite of many obstacles memories of all types continue to grow in speed and density. Particularly noteworthy are the 64-K **MOS dynamic random-access memories**, the existence of electrically erasable PROMs and the forthcoming 1-megabit bubble memory chips. Discussed are newly announced available and coming memory devices.

22/3,AB/19 (Item 7 from file: 8)

01/22/2003

DIALOG(R)File 8:Ei Compendex(R)

01081388
E.I. Monthly No: EI8112098415
E.I. Yearly No: EI81024314
Title: EPITAXIAL LAYER BLOCKS UNWANTED CHARGE IN MOS RAMs.
Author: Mohan Rao, G. R.; White, L. S. Jr.; Gossen, Richard N.
Corporate Source: Tex Instrum Inc, Houston
Source: Electronics v 54 n 13 Jun 30 1981 p 103-105
Publication Year: 1981
CODEN: ELECAD ISSN: 0013-5070
Language: ENGLISH
Abstract: With **dynamic MOS random-access memories** now up to the 64-K level, minor problems have become major ones. Superfluous charge, which can be caused by the rapid switching of address signals or by alpha particles, is one of these problems. The method of controlling this unwanted charge is described. A lightly doped epitaxial layer permits the use of a heavily doped substrate that sweeps away error-causing superfluous minority carriers.

22/3,AB/20 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00740771
E.I. Monthly No: EI7809064349
E.I. Yearly No: EI78020994
Title: DYNAMIC M. O. S. R. A. M. S.
Author: Proebsting, Robert
Corporate Source: Mostek Corp
Source: New Electronics v 10 n 18 Sep 20 1977 p 46, 50, 54, 56
Publication Year: 1977
CODEN: NWELAC ISSN: 0047-9624
Language: ENGLISH
Abstract: The evolution of **dynamic MOS random access memories** (RAM's) is outlined. Address multiplexing and timing considerations of multiplexed address devices are discussed. Static and dynamic sense problems, and the benefits resulting from the use of dynamic sense amplifiers are evaluated.

22/3,AB/21 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00702745
E.I. Monthly No: EI7803016713
E.I. Yearly No: EI78021187
Title: D10 SWITCHING SYSTEM SEMICONDUCTOR MAIN MEMORY EQUIPMENT.
Author: Hiyama, Yasuhiro; Ohnishi, Noboru; Takagi, Shigeru; Ishikawa, Tsutomu
Corporate Source: Nippon Telegr & Teleph Public Corp, Musashino, Jpn
Source: Review of the Electrical Communication Laboratories (Tokyo) v 25 n 5-6 May-Jun 1977 p 411-420
Publication Year: 1977
CODEN: RELTAN ISSN: 0418-6338
Language: ENGLISH
Abstract: The paper describes the design and evaluation of a 4k-bit n-channel **dynamic MOS random access memory**

having an access time of 300 ns. It is shown that processing performance, space factor, power consumption and manufacturing cost of such memory equipment are substantially improved in comparison with the conventional core memory equipment. 6 refs.

22/3,AB/22 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00659120
E.I. Monthly No: EI7710072599
E.I. Yearly No: EI77021343
Title: N CHANNEL MOS DYNAMIC 4K RAM.
Author: Shirato, Hajime; Matsue, Shigeki
Corporate Source: Nippon Electr Co, Nakahara, Kawasaki, Jpn
Source: Denshi Tokyo n 15 1976 p 12-14
Publication Year: 1976
CODEN: DETODX ISSN: 0285-1903
Language: ENGLISH
Abstract: Described is an n-channel 4K **dynamic MOS random-access memory** (RAM) using a 3 transistor/bit cell. This chip requires only a single clock and internally generates the timing required. Except for the single high voltage clock, all inputs and the output are TTL compatible.

22/3,AB/23 (Item 11 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00265346
E.I. Monthly No: EI7211008183
Title: DESIGN FOR A HIGH-SPEED M. O. S. ASSOCIATIVE MEMORY.
Author: Lea, R. M.
Corporate Source: Brunel Univ, Uxbridge, Middlesex, Engl
Source: Electronics Letters v 8 n 15 Jul 27 1972 p 391-393
Publication Year: 1972
CODEN: ELLEAK ISSN: 0013-5194
Language: ENGLISH
Abstract: An experimental 64-bit MOS associative memory has been developed from a limit-case design study. Speeds in excess of 50 MHz are reported at a cost per bit that could approach eight times that for a conventional **MOS dynamic random-access memory**. The design of the basic associative memory cell is described.

22/3,AB/24 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

09567441 Genuine Article#: 419AN Number of References: 97
Title: Device scaling limits of Si MOSFETs and their application dependencies (ABSTRACT AVAILABLE)
Author(s): Frank DJ (REPRINT) ; Dennard RH; Nowak E; Solomon PM; Taur Y; Wong HSP
Corporate Source: IBM Corp,Thomas J Watson Res Ctr,Yorktown Heights//NY/10598 (REPRINT); IBM Corp,Thomas J Watson Res Ctr,Yorktown Heights//NY/10598
Journal: PROCEEDINGS OF THE IEEE, 2001, V89, N3,SI (MAR), P259-288
ISSN: 0018-9219 Publication date: 20010300

Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394 USA
Language: English Document Type: ARTICLE
Abstract: This paper presents the current state of understanding of the factors that limit the continued scaling of Si complementary metal-oxide-semiconductor (CMOS) technology and prov ides an analysis of the ways in which application-related considerations enter into the determination of these limits. The physical origins of these limits are primarily in the tunneling currents. which leak through the various barriers in a MOS field-effect transistor (MOSFET) when it becomes very small. and in the thermally generated subthreshold currents. The dependence of these leakages on MOSFET geometry? and structure is discussed along with design criteria for minimizing short-channel effects and other issues related to scaling. Scaling limits due to these leakage currents arise from application constraints related to power consumption and circuit functionality. We describe her; these constraints work out for some of the most important application classes: dynamic random access memory (DRAM, static random access memory (SRAM), low-power portable det ices, and moderate and high-performance CMOS logic. As a summary: we provide a table of our estimates of the scaling limits for various applications and device types. The end result is that there is no single end point for scaling. but that instead there are many end points, each optimally adapted to its particular applications.

22/3,AB/25 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

09392358 Genuine Article#: 400VP Number of References: 9
Title: Channel engineering using RTA prior to the gate oxidation for high density DRAM with single gate CMOS technology (ABSTRACT AVAILABLE)
Author(s): Son JH; Lee SH; Lee JS (REPRINT) ; Lee Y
Corporate Source: Hyundai Micro Elect Co Ltd,R&D Div,1 Hyangjeong Dong/Cheongju 360480//South Korea/ (REPRINT); Hyundai Micro Elect Co Ltd,R&D Div,Cheongju 360480//South Korea/
Journal: SOLID-STATE ELECTRONICS, 2001, V45, N1 (JAN), P7-12
ISSN: 0038-1101 Publication date: 20010100
Publisher: PERGAMON-ELSEVIER SCIENCE LTD, THE BOULEVARD, LANGFORD LANE, KIDLINGTON, OXFORD OX5 1GB, ENGLAND
Language: English Document Type: ARTICLE
Abstract: A non-uniform lateral boron profile along the channel width is observed in a buried-channel p-MOSFET and a memory cell transistor when BF2 implantation is applied at the dose of similar to 10(13) cm(-2) to form a channel. SIMS profile analysis and two-dimensional simulation results show that this abnormal profile is formed by transient enhanced diffusion (TED) due to BF2 implantation damage during gate oxidation process. It is Found that RTA process just prior to the gate oxidation is useful to eliminate the TED of boron so that inverse narrow width effect, short channel effect and threshold voltage fluctuation are remarkably improved in a buried-channel p-MOSFET. In addition, the RTA process can also reduce BF2 implantation dose without decreasing threshold voltage by the suppression of boron diffusion in a cell transistor. Therefore. the retention time of DRAM can be enhanced by reducing space charge region field in a cell transistor due to lower boron concentration compared with a conventional device. (C) 2001 Published by Elsevier Science Ltd. All rights reserved.

22/3,AB/26 (Item 3 from file: 34)

01/22/2003

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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08111431 Genuine Article#: 247ZF Number of References: 26
Title: Physics and characterization of transient effects in SOI transistors (ABSTRACT AVAILABLE)
Author(s): Lacaita AL (REPRINT) ; Perron LM
Corporate Source: POLITECN MILAN,DEI, PIAZZA L DA VINCI 32/I-20133 MILAN//ITALY/ (REPRINT); STMICROELECT,/I-20041 AGRATE BRIANZA//ITALY/
Journal: MICROELECTRONIC ENGINEERING, 1999, V48, N1-4 (SEP), P319-326
ISSN: 0167-9317 Publication date: 19990900
Publisher: ELSEVIER SCIENCE BV, PO BOX 211, 1000 AE AMSTERDAM, NETHERLANDS
Language: English Document Type: ARTICLE
Abstract: The work reviews the physics of transient floating-body effects in SOI devices and gives some examples of their impact on circuit performance.

22/3,AB/27 (Item 1 from file: 434)
DIALOG(R)File 434:SciSearch(R) Cited Ref Sci
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09414625 Genuine Article#: T9728 Number of References: 3
Title: A FAULT MODEL FOR MULTIVALUED **NMOS DYNAMIC RANDOM-ACCESS MEMORIES**
Author(s): NAIDU RV; MAHAPATRA S
Corporate Source: INDIAN INST TECHNOL,ADV CTR RES ELECTR/BOMBAY 400076//INDIA/
Journal: MICROELECTRONICS AND RELIABILITY, 1989, V29, N2, P137-143
Language: ENGLISH Document Type: ARTICLE

22/3,AB/28 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
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14959367 PASCAL No.: 01-0112008
Dependence of Subthreshold Hump and Reverse Narrow Channel Effect on the Gate Length by Suppression of Transient Enhanced Diffusion at Trench Isolation Edge
JUNG Jong-Wan; KIM Jong-Min; SON Jeong-Hwan; LEE Youngjong
Hyundai Electronics Industries Co., Ltd., 1, Hyangjeong-dong, Hungduk-gu, Cheongju, 361-480, Korea
Journal: Japanese Journal of Applied Physics, Part I : Regular papers, short notes & review papers, 2000-04-30, 39 (4B) 2136-2140
Language: English
For the first time to our knowledge, we have shown that subthreshold hump and reverse narrow channel effect characteristics depend on the gate length, and that the hump strength has a peak point at the gate length where the threshold voltage is highest. In order to explain these effects, we proposed a new model in which the boron transient enhanced diffusion at the trench isolation edge is more suppressed than that at the middle channel. The simulation results using the proposed model agreed well with the experimental results.

22/3,AB/29 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal
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01/22/2003

08661063 PASCAL No.: 89-0210283
power reduction methods for **NMOS dynamic random access memories**
VENKATAPATHI NAIDU R; MAHAPATRA S
Indian inst. technology, Bombay 400076, India
Journal: Microelectronics and Reliability, 1988, 28 (6) 877-883
Language: English
On propose des methodes de reduction de puissance pour les memoires a acces direct dynamiques NMOS afin de reduire la dissipation de puissance. Quand la densite de bits croit, la dissipation de puissance croit. Dans la conception des memoires a acces direct dynamiques de l'ordre du megabit, une consideration importante est la tension d'alimentation de puissance, qui doit etre fixee en fonction de la dissipation de puissance, de la fiabilite, qui depend des effets de champ intense, dus a la petitesse des dispositifs, et de la marge de fonctionnement de la cellule de memoire. Discussion de la dissipation de puissance dans les decodeurs et circuits integres NMOS des memoires a acces direct dynamiques de l'ordre du Mbit. Realisation par un circuit VLSI prototype, proprietes fondamentales des

26/3,AB/1 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

11093639 Genuine Article#: 607ER Number of References: 55
Title: Challenges and future directions for the scaling of **dynamic random-access memory** (DRAM) (ABSTRACT AVAILABLE)
Author(s): Mandelman JA (REPRINT) ; Dennard RH; Bronner GB; DeBrosse JK; **Divakaruni R**; Li Y; Radens CJ
Corporate Source: IBM Corp,Microelect Div, E Fishkill Facil,Route 52/Hopewell Jct//NY/12533 (REPRINT); IBM Corp,Microelect Div, E Fishkill Facil,Hopewell Jct//NY/12533; IBM Corp,Div Res, Thomas J Watson Res Ctr,Yorktown Hts//NY/10598; IBM Corp,Microelect Div, Burlington Facil,Essex Jct//VT/05452
Journal: IBM JOURNAL OF RESEARCH AND DEVELOPMENT, 2002, V46, N2-3 (MAR-MAY), P187-212
ISSN: 0018-8646 Publication date: 20020300
Publisher: IBM CORP, OLD ORCHARD RD, ARMONK, NY 10504 USA
Language: English Document Type: ARTICLE
Abstract: Significant challenges face DRAM scaling toward and beyond the 0.10-mum generation. Scaling techniques used in earlier generations for the array-access transistor and the storage capacitor are encountering limitations which necessitate major innovation in electrical operating mode, structure, and processing. Although a variety of options exist for advancing the technology, such as low-voltage operation, vertical **MOSFETs**, and novel capacitor structures, uncertainties exist about which way to proceed. This paper discusses the interrelationships among the DRAM scaling requirements and their possible solutions. The emphasis is on trench-capacitor DRAM technology.

26/3,AB/2 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

11049630 Genuine Article#: 602GQ Number of References: 10
Title: 1.5-V single work-function W/WN/n(+)-poly gate CMOS device design with 110-nm buried-channel **PMOS** for 90-nm vertical-cell DRAM (ABSTRACT AVAILABLE)
Author(s): Rengarajan R (REPRINT) ; He BY; Ransom C; Choi CJ; Ramachandran R; Yang HN; Butt S; Halle S; Yan W; Lee K; Chudzik M; Parks C; Massey JG; La Rosa G; Li YJ; Radens C; **Divakaruni R**; Crabbe E
Corporate Source: IBM Microelect Semicond Res & Dev Ctr,Infineon Technol,Hopewell Jct//NY/12533 (REPRINT); IBM Microelect Semicond Res & Dev Ctr,Infineon Technol,Hopewell Jct//NY/12533
Journal: IEEE ELECTRON DEVICE LETTERS, 2002, V23, N10 (OCT), P621-623
ISSN: 0741-3106 Publication date: 20021000
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394 USA
Language: English Document Type: ARTICLE
Abstract: This letter reports on 1.5-V single work-function W/WN/n(+)-poly gate CMOS transistors for high-performance stand-alone **dynamic random access memory** (DRAM) and low-cost low-leakage embedded DRAM applications. At V-dd Of 1.5-V and 25 degreesC, drive currents of 634 muA/mum for 90-nm L-gate **NMOS** and 208 muA-mum for 110-mn L-gate buried-channel **PMOS** are achieved at 25 pA/mum off-state leakage. Device performance of this single work function technology is comparable to published low leakage 1.5-V dual work-function technologies and 25% better than previously reported 1.8-V single work-function technology. Data illustrating hot-carrier

immunity of these devices under high electric fields is also presented. Scalability of single work-function CMOS device design for the 90-nm DRAM generation is demonstrated.

26/3,AB/3 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

11165208 PASCAL No.: 93-0674463
The current-carrying corner inherent to trench isolation
BRYANT A; HAENSCH W; GEISSLER S; **MANDELMAN J**; POINDEXTER D; STEGER M
IBM, technology products, Essex Junction VT 05452, USA
Journal: IEEE electron device letters, 1993, 14 (8) 412-414
Language: English

In this paper it is shown for the first time how the characteristics of the corner **MOSFET** inherent to trench isolation can be extracted from hardware measurements and how the corner device must be taken into account when extracting **MOSFET** channel characteristics. For NFET's it is found that the corner's threshold voltage, substrate sensitivity, and sensitivity to well doping are all smaller than the channel's. The results imply that for low standby power logic applications requiring high performance, it may become necessary to locally control the well doping at the corner. However, the corner's reduced substrate sensitivity and width independence can provide a significant advantage in a DRAM cell

34/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6747707 INSPEC Abstract Number: B2000-12-1265D-017, C2000-12-5320G-004
Title: Process integration trends for embedded DRAM
Author(s): Takato, H.; Koike, H.; Yoshida, T.; Ishiuchi, H.
Author Affiliation: Microelectron. Eng. Lab., Toshiba Corp., Yokohama, Japan
Conference Title: ULSI Process Integration. Proceedings of the First International Symposium (Electrochemical Society Proceedings Vol.99-18) p.107-19
Editor(s): Claeys, C.L.; Iwai, H.; Bronner, G.; Fair, R.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1999 Country of Publication: USA xiii+386 pp.
ISBN: 1 56677 241 9 Material Identity Number: XX-2000-00269
Conference Title: Proceedings of ULSI Process Integration
Conference Sponsor: Electrochem. Soc
Conference Date: 17-22 Oct. 1999 Conference Location: Honolulu, HI, USA
Language: English
Abstract: Issues and development trends with respect to embedded DRAM (**eDRAM**) technology are reviewed by referring to real implementations for 0.5 mu m, 0.35 mu m and 0.25 mu m generations. Chip performance has been progressively improved throughout the development of 0.5 mu m, 0.35 mu m and 0.25 mu m **eDRAM** . However, the number of process steps has increased compared to that for commodity DRAM. To avoid this problem and achieve the highest possible device performance, future directions for embedded DRAM technologies, including **MOSFET** structure, memory cells, process cost and performance, are also discussed. For the **MOSFET** structure, the logic-based **MOSFET** process offers more advantages than the DRAM-based one for future **eDRAM** generations. For memory cell structure, the trench cell is expected to be more useful for future **eDRAM** compared to the stacked cell. In order to combine the trench cell and logic based **MOSFET** process, a new embedded DRAM technology is proposed. This process technology provides full process compatibility with high performance logic and a minimum number of process steps, resulting in low process cost and short TAT (turnaround time). A DRAM array macro has been fabricated using this technology with Co salicide, dual work function gate and aluminum **bit-line** processes, and excellent DRAM retention characteristics have been confirmed using a negative **word-line** bias scheme.
Subfile: B C

34/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6737400 INSPEC Abstract Number: B2000-12-0520F-010
Title: Plasma enhanced chemical vapor deposition Si-rich silicon oxynitride films for advanced self-aligned contact oxide etching in sub-0.25 mu m ultralarge scale integration technology and beyond
Author(s): Jeong-Ho Kim; Jae-Seon Yu; Ja-Chun Ku; Choon-Kun Ryu; Su-Jin Oh; Si-Bum Kim; Jin-Woong Kim; Jeong-Mo Hwang; Su-Youb Lee; Kouichiro, I.
Author Affiliation: Semicond. Adv. Res. Div., Hyundai Electron. Ind. Co. Ltd., South Korea
Journal: Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films) Conference Title: J. Vac. Sci. Technol. A, Vac. Surf. Films (USA)

vol.18, no.4, pt.1-2 p.1401-10
Publisher: AIP for American Vacuum Soc,
Publication Date: July-Aug. 2000 Country of Publication: USA
CODEN: JVTAD6 ISSN: 0734-2101
SICI: 0734-2101(200007/08)18:4:1/2L.1401:PECV;1-2
Material Identity Number: D746-2000-005
U.S. Copyright Clearance Center Code: 0734-2101/2000/18(4)/1401(10)/$15.00
Conference Title: 46th National Symposium of the American Vacuum Society. Vacuum, Surfaces, and Films
Conference Date: 25-29 Oct. 1999 Conference Location: Seattle, WA, USA
Language: English
Abstract: We intentionally introduced excessive Si during the SiO/sub x/N/sub y/ film deposition in order to increase the etch selectivity-to-SiO/sub x/N/sub y/ for advanced self-aligned contact (SAC) etching in sub-0.25 mu m ultralarge scale integration devices. The SiO/sub x/N/sub y/ layer was deposited at a conventional plasma enhanced chemical vapor deposition chamber by using a mixture of SiH/sub 4/, NH/sub 3/, N/sub 2/O, and He. The gas mixing ratio was optimized to get the best etch selectivity and low leakage current. The best result was obtained at 10% Si-SiO/sub x/N/sub y/. In order to employ SiO/sub x/N/sub y/ film as an insulator as well as a SAC barrier, the leakage current of SiO/sub x/N/sub y/ film was evaluated so that SiO/sub x/N/sub y/ may have the low leakage current characteristics. The leakage current of 10% Si-SiO/sub x/N/sub y/ film was 7*10/sup -9/ A/cm/sup 2/. Besides, the Si-rich SiO/sub x/N/sub y/ layer excellently played the roles of antireflection coating for **word line** and **bit line** photoresist patterning and sidewall spacer to build a **metal-oxide-semiconductor transistor** as well as a SAC oxide etch barrier. The contact oxide etching with the Si-rich SiO/sub x/N/sub y/ film was done using C/sub 4/F/sub 8//CH/sub 2/F/sub 2//Ar in a dipole ring magnet plasma. As the C/sub 4/F/sub 8/ flow rate increases, the oxide etching selectivity-to-SiO/sub x/N/sub y/ increases but etch stop tends to happen. Our optimized contact oxide etch process showed the high selectivity to SiO/sub x/N/sub y/ larger than 25 and a wide process window (>or=5 sccm) for the C/sub 4/F/sub 8/ flow rate. When the Si-rich SiO/sub x/N/sub y/ SAC process was applied to a gigabit **dynamic random access memory** of cell array, there was no electrical short failure between conductive layers.
Subfile: B

34/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

03854525 INSPEC Abstract Number: B91023599
Title: Buried **bit-line** cell for 64 Mb DRAMs
Author(s): Kohyama, Y.; Yamamoto, T.; Sudo, A.; Watanabe, T.; Tanaka, T.
Author Affiliation: Toshiba Corp., Kawasaki, Japan
Conference Title: 1990 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.90CH2874-6) p.17-18
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA xvii+143 pp.
U.S. Copyright Clearance Center Code: CH2874-6/90/0000-0017$01.00
Conference Sponsor: IEEE; Japan Soc. Appl. Phys
Conference Date: 4-7 June 1990 Conference Location: Honolulu, HI, USA
Language: English
Abstract: The authors propose a buried **bit-line** (BBL) stacked capacitor cell structure for high-density **dynamic random**

access memories (DRAMs). The cell area can be reduced to as small as 8.7F/sup 2/, where F is the lithographic feature size. A 2.25- mu m/sup 2/ cell area is achieved using a 0.51- mu m feature size. A 1.4- mu m/sup 2/ cell area is attainable using a 0.4- mu m feature size. The memory-cell vertical size (2F) includes a line and space for a trench isolation pattern in which the buried **bit-line** is formed. The horizontal size (4F+a) includes two **word-line** line and space pairs and a **word-line** to **bit-line** contact alignment tolerance denoted by a. A storage node contact is self-aligned to the **word-line** . Since the a is considered to be less than F/2, a cell area of less than 9F/sup 2/ is realized. If the **bit-line** contact is also self-aligned to the **word-line**, an 8F/sup 2/ cell area can in theory be realized.
Subfile: B

34/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

01511422 INSPEC Abstract Number: B80024087
Title: Fabrication of V-**MOS** or U-**MOS random-access memory** cells with a self-aligned **word line**
Author(s): Chang, T.S.; Ogura, S.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.22, no.7 p.2768-71
Publication Date: Dec. 1979 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: A self-aligned **word line** for V-**MOS** and U-**MOS random-access memories** reduces the cell areas, **bit line** capacitance and **word line** resistance.
Subfile: B

34/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

01422567 INSPEC Abstract Number: B79047285, C79030068
Title: One-device cells for **dynamic random-access memories**: a tutorial
Author(s): Rideout, V.L.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Journal: IEEE Transactions on Electron Devices vol.ED26, no.6 p. 839-52
Publication Date: June 1979 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
Language: English
Abstract: The evolutionary development of one-device cells for **dynamic random-access memory** (RAM) integrated circuits is described. From an examination of the areal layout (planar top view) and the cross section (vertical topography), various memory cells are compared in a systematic manner. Structural features such as contact via formation, **bit-line** and **word-line** pitch, metal step coverage, and cell placement along the **bit line** are also considered. Some new dynamic RAM cell concepts such as doubly doped storage capacitors, self-registering contacts, and **VMOS** FET's are discussed. From an examination of commercially available dynamic RAM chips, a basic lithographic groundrule was determined.

01/22/2003

Subfile: B C

34/3,AB/6 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS
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1192950 NTIS Accession Number: PB85-226090
One-M bit **NMOS** Dynamic RAM
Sakui, K. ; Miyawaki, N. ; Nakayama, R.
Toshiba Corp., Tokyo (Japan).
Corp. Source Codes: 021559000
c1985 4p
Languages: Japanese
Journal Announcement: GRAI8521
Text in Japanese.
Included in Toshiba Review, v40 n6 p478-481 1985.
NTIS Prices: (Order as PB85-226074, PC E05/MF E01)
The high performance 1-M words x 1-bit **NMOS** dynamic RAM has been developed by using proprietary BOX (buried oxide) isolation and two-level aluminum metalization techniques. The memory cell, adopting a novel folded capacitor cell structure realizing a large cell capacitance (70 fF), enables the RAM to operate with large noise margin and high alpha particle immunity. In order to realize high-speed and low-power operation, the RAM utilises the reduction of **word line** resistance (by means of second-level Al interconnection), high-speed sense amplifier system, partial activation scheme of memory cell arrays, and reduction of **bit -line** length. It has achieved 30 ns of CAS access time and 270 mW of active power dissipation at 260 ns cycle time.

34/3,AB/7 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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06057013
E.I. No: EIP02216955097
Title: A capacitor-less 1T-DRAM cell
Author: Okhonin, S.; Nagoga, M.; Sallese, J.M.; Fazan, P.
Corporate Source: LEG Swiss Federal Inst. of Technol., CH-1015 Lausanne, Switzerland
Source: IEEE Electron Device Letters v 23 n 2 February 2002. p 85-87
Publication Year: 2002
CODEN: EDLEDZ ISSN: 0741-3106
Language: English
Abstract: A simple true 1 transistor **dynamic random access memory** (DRAM) cell concept is proposed for the first time, using the body charging of partially-depleted SOI devices to store the logic "1" or "0" binary states. This cell is two times smaller in area than the conventional 8F**2 1T/1C DRAM cell and the process of its manufacturing does not require the storage capacitor fabrication steps. This concept will allow the manufacture of simple low cost DRAM and embedded DRAM chips for 100 and sub-100 nm generations. 12 Refs.

34/3,AB/8 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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05587584
E.I. No: EIP00065217411

01/22/2003

Title: Robust 8F**2 ferroelectric RAM cell with depletion device (DeFeRAM)
Author: Braun, Georg; Hoenigschmid, Heinz; Schlager, Tobias; Weber, Werner
Corporate Source: Infineon Technologies AG, Munich, Ger
Conference Title: The 1999 Symposium on VLSI Circuits
Conference Location: Kyoto, Jpn Conference Date: 20990617-20990619
E.I. Conference No.: 56947
Source: IEEE Journal of Solid-State Circuits v 35 n 5 2000. p 691-696
Publication Year: 2000
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: This paper describes an area-penalty-free, leakage-compensated, and noise-immune 8F**2 cell design suitable for high-density, low-power ferroelectric RAM (FeRAM) generations. The new concept features a 1T1C ferroelectric memory cell containing an additional depletion device (DeFeRAM) controlled by the passing **word line** in a folded **bit-line** architecture. The depletion device permits the use of a common cell plate at intermediate voltage level. A highly reliable three-level **word-line** driver circuit design is discussed. (Author abstract) 7 Refs.

34/3,AB/9 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05583444
E.I. No: EIP00065217433
Title: 0.5- mu m, 3-V, 1T1C, 1-Mbit FRAM with a variable reference **bit-line** voltage scheme using a fatigue-free reference capacitor
Author: Ogiwara, Ryu; Tanaka, Sumio; Itoh, Yasuo; Miyakawa, Tadashi; Takeuchi, Yoshiaki; Doumae, Sumiko Mano; Takenaka, Hiroyuki; Kunishima, Iwao; Shuto, Susumu; Hidaka, Osamu; Ohtsuki, Sumito; Tanaka, Shin-ichi
Corporate Source: Toshiba Corp, Yokohama, Jpn
Source: IEEE Journal of Solid-State Circuits v 35 n 4 2000. p 545-551
Publication Year: 2000
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: A 0.5- mu m, 3-V operated, 1T1C, 1-Mbit FRAM with 160-ns access time has been developed. In FRAM, a reference voltage design using a ferroelectric capacitor is difficult because of the degradation due to fatigue, a chip-to-chip variation, and a temperature dependence. A variable reference voltage scheme is generated to solve this problem, boosting a fatigue-free and temperature-independent **MOS** reference capacitance by a driver. The driver is operated from a compact reference voltage generator that provides 32 equally divided voltages and occupies only half the layout area of a conventional one. During sense operation, memory-cell capacitance C//f//e//r//r is larger than reference-cell capacitance C//M//O//S. A double **word-line** pulse scheme has also been developed to eliminate a **bit-line** capacitance imbalance in the **bit-line** pairs, where a memory cell and a reference cell are separated from the **bit-line** pairs during sense operation. A six-order improvement in imprint lifetime has been achieved by the new scheme. (Author abstract) 5 Refs.

34/3,AB/10 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05050777
E.I. No: EIP98074264245
Title: 3.6 mW 1.4 V SRAM with non-boosted, vertical bipolar **bitline** contact memory cell
Author: Sato, H.; Nagaoka, H.; Honda, H.; Maki, Y.; Wada, T.; Arita, Y.; Tsutsumi, K.; Yamada, M.
Corporate Source: Mitsubishi Electric Corp, Hyogo, Jpn
Conference Title: Proceedings of the 1998 IEEE 45th International Solid-State Circuits Conference, ISSCC
Conference Location: San Francisco, CA, USA Conference Date: 19980205-19980207
E.I. Conference No.: 48558
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1998. IEEE, Piscataway, NJ, USA,98CH36156. p 352-353, 463 PAPER SP 22.3
Publication Year: 1998
CODEN: DTPCDE ISSN: 0193-6530
Language: English
Abstract: Low-voltage static **random access memory** (SRAM) operating at less than 3 V are used for handy terminals, however, demand for lower-voltage operation has increased. It is difficult to reduce operating voltage below 2.5 V with the conventional low-power SRAM with 4 **nMOS**-transistor cell. Although a full CMOS cell or a boosted **word line** technique can reduce operating voltage, they have certain problems. A 256 kb, low-power SRAM using a bipolar **bit line** contact (BBC) memory cell used to solve these problems which features small cell, low-operating voltage, low power distribution and fast access is presented. 2 Refs.

34/3,AB/11 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04970705
E.I. No: EIP98034104375
Title: Low temperature metal-based cell integration technology for gigabit and embedded DRAMs
Author: Yoshida, Makoto; Kumauchi, Takahiro; Kawakita, Keizo; Ohashi, Naofumi; Enomoto, Hiroyuki; Umezawa, Tadashi; Yamamoto, Naoki; Asano, Isamu ; Tadaki, Yoshitaka
Corporate Source: Hitachi Ltd, Tokyo, Jpn
Conference Title: Proceedings of the 1997 International Electron Devices Meeting
Conference Location: Washington, DC, USA Conference Date: 19971207-19971210
E.I. Conference No.: 48095
Source: Proceedings of the IEEE Hong Kong Electron Devices Meeting 1997. IEEE, Piscataway, NJ, USA,97CH36103. p 41-44
Publication Year: 1997
CODEN: 002525
Language: English
Abstract: An advanced memory cell structure with poly/metal **word lines** and metal **bit lines** is proposed. The thermal processes are carefully designed for the metal-based cell to be consistent with narrow gap filling, wet cleaning, planarity, and the contact process. The extremely low temperature process also helps suppress the short channel effect of the **MOS** transistors. The fully self-aligned contact and via-hole technology provides the minimum memory cell area. This technology is promising for future gigabit DRAMs and embedded DRAMs. (Author abstract)

01/22/2003

6 Refs.

34/3,AB/12 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04624882
E.I. No: EIP97023516176
Title: 0.23 mu m**2 double self-aligned contact cell for gigabit DRAMs with a Ge-added vertical epitaxial Si pad
Author: Koga, H.; Kasai, N.; Hada, H.; Tatsumi, T.; Mori, H.; Iwao, S.; Saino, K.; Yamaguchi, H.; Nakajima, K.; Yamada, Y.; Tokunaga, K.; Hirasawa, S.; Yoshida, K.; Nishizawa, A.; Hashimoto, T.; et al
Corporate Source: NEC Corp, Kanagawa, Jpn
Conference Title: Proceedings of the 1996 IEEE International Electron Devices Meeting
Conference Location: San Francisco, CA, USA Conference Date: 19961208-19961211
E.I. Conference No.: 46059
Source: Technical Digest - International Electron Devices Meeting 1996. IEEE, Piscataway, NJ, USA,96CH35961. p 589-592
Publication Year: 1996
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: A new stacked capacitor memory cell with folded **bit-line** arrangement has been developed using a double self-aligned contact technology. By using a combination of a vertical epitaxial growth Si pad and Si//3N//4 caps as etch stop layers on both the **bit-lines** and **word-lines**, the cell area using 0.15 mu m design rule can be reduced to 0.23 mu m**2 with 0.1 mu m alignment tolerance. Through addition of germanium (Ge) to the Si pad, the controllability of epitaxially grown Si pad features can be improved, resulting in an increase in the growth rate ratio of perpendicular to lateral directions by a factor of 4 and a decrease in resistance of the epi pad from 5k Omega to 1k Omega . (Author abstract) 6 Refs.

34/3,AB/13 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04313529
E.I. No: EIP95122958382
Title: Current direction sense technique for multi-port SRAMs
Author: Izumikawa, Masanori; Yamashina, Masakazu
Corporate Source: NEC Corp, Kanagawa, Jpn
Conference Title: Proceedings of the 1995 Symposium on VLSI Circuits
Conference Location: Kyoto, Jpn Conference Date: 19950608-19950610
E.I. Conference No.: 44078
Source: IEEE Symposium on VLSI Circuits, Digest of Technical Papers 1995. IEEE, Piscataway, NJ, USA,95CH35780. p 23-24
Publication Year: 1995
CODEN: 85PXA5
Language: English
Abstract: Single-end sense amplifiers which do not require a reference voltage would be most desirable for multi-port SRAMs. This paper describes a current-direction sense circuit which transforms current direction into a logic value. It operates four times faster than a CMOS inverter, and with it, it is possible to produce single-end 200 MHz 64 kb SRAMs whose total power consumption is nearly as low as that required for the memory cell

currents alone in conventional SRAMs. Also presented is a write **bit-line** and **word-line** swing. When this circuit is applied to be used in a 200 MHz 64 kb SRAM, it is possible to reduce by one-third the power consumption required for **bit-line** driving and pseudo-read cell current (0.25 mu m CMOS). 1 Refs.

34/3,AB/14 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04001605
E.I. No: EIP94122451194
Title: Vertical Phi -shape transistor (V Phi T) cell for 1Gbit DRAM and beyond
Author: Maeda, S.; Maegawa, S.; Ipposhi, T.; Nishimura, H.; Kuriyama, H.; Tanina, O.; Inoue, Y.; Nishimura, T.; Tsubouchi, N.
Corporate Source: ULSI Lab Mitsubishi Electric Corp, Hyogo, Jpn
Conference Title: Proceedings of the 1994 Symposium on VLSI Technology
Conference Location: Honolulu, HI, USA Conference Date: 19940607-19940609
E.I. Conference No.: 21361
Source: Digest of Technical Papers - Symposium on VLSI Technology 1994. IEEE, Piscataway, NJ, USA,94CH3433-0. p 133-134
Publication Year: 1994
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: We propose a Vertical Phi -shape Transistor (V Phi T) cell for 1Gbit DRAM and beyond. The V Phi T is a vertical **MOSFET** whose gate surrounds its channel region like a Greek alphabet Phi . It is built by penetration of the gate electrode (equals **word line**) which has been formed beforehand. Application of the V Phi T for DRAM cell brings about cell size reduction to 50% and process simplification of about 10% at least, mainly because its **bit line** contact and the V Phi T are vertically aligned and storage node contact is eliminated. We have indicated that the V Phi T is an interesting candidate for the gigabit DRAM in view of size, cost and performance. (Author abstract) 12 Refs.

34/3,AB/15 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03894125
E.I. No: EIP94071336921
Title: Design rule relaxation approach for high-density DRAMs
Author: Saeki, Takanori; Kakehashi, Eiichiro; Mori, Hidemitu; Koga, Hiroki; Noda, Kenji; Fujita, Mamoru; Sugawara, Hiroshi; Nagata, Kyoichi; Nishimoto, Shozo; Murotani, Tatsunori
Corporate Source: NEC Corp, Sagamihara-shi, Jpn
Source: IEICE Transactions on Electronics v E77-C n 3 Mar 1994. p 406-415
Publication Year: 1994
CODEN: IELEEJ ISSN: 0916-8524
Language: English
Abstract: A design rule relaxation approach is one of the most important requirements for high density DRAMs. The approach relaxes the design rule of a element in comparison with the memory cell size and provides high density DRAMs with the minimum development of a scaled-down **MOS** structure and a fine patterning lithography process. This paper describes two design rule relaxation approaches, a close-packed folded (CPF) **bit-line** cell array layout and a Boosted Dual **Word-**

Line scheme. The CPF cell array provides 1.26 times wider active area pitch and maximum 1.5 times wider isolation width. The Boosted Dual **Word-Line** scheme provides 2**n times wider 1st Al pitch on memory cell array, double **word-line** driver pitch and 1.5 times larger design rule for 1st Al and contacts under 1st Al. Especially wide design rule of the Boosted Dual **Word-Line** scheme provides several times depth of focus (DOF) for 1st Al wiring which gives several times higher storage node and larger capacitance for capacitor over **bit-line** (COB) stacked capacitor cells. These approaches are successfully implemented in a 4 Mb DRAM test chip with a 0.9 multiplied by 1.8 mu m**2 memory cell. (Author abstract) 14 Refs.

34/3,AB/16 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03783613
E.I. No: EIP94011186903
Title: Single-**bit-line** cross-point cell activation (SCPA) architecture for ultra-low-power SRAM's
Author: Ukita, Motomu; Murakami, Shuji; Yamagata, Tadato; Kurijama, Hirotada; Nishimura, Yasumasa; Anami, Kenji
Corporate Source: Mitsubishi Electric Corp, Itami City, Jpn
Source: IEEE Journal of Solid-State Circuits v 28 n 11 Nov 1993. p 1114-1118
Publication Year: 1993
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: This paper describes a single-**bit-line** cross-point cell activation (SCPA) architecture, which has been developed to reduce active power consumption and to avoid increase in the size of high-density SRAM chips, such as 16-Mb SRAM's and beyond. A new **PMOS** precharging boost circuit, introduced to realize the single-**bit-line** structure, is also discussed. This circuit is suitable for operation under low-voltage power supply conditions. The SCPA architecture with the new **word-line** boost circuit is demonstrated with the experimental device, which is fabricated by 0.4- mu m CMOS wafer process technology. (Author abstract) 3 Refs.

34/3,AB/17 (Item 11 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03394565
E.I. Monthly No: EI9203031448
Title: A 33-ns 64-Mb DRAM.
Author: Oowaki, Yukihito; Tsuchida, Kenji; Watanabe, Yohji; Takashima, Daisaburo; Ohta, Masako; Nakano, Hiroaki; Watanabe, Shigeyoshi; Nitayama, Akihiro; Horiguchi, Fumio; Ohuchi, Kazunori; Masuoka, Fujio
Corporate Source: Toshiba Corp, Saiwai-ku, Kawasaki, Japan
Source: IEEE Journal of Solid-State Circuits v 26 n 11 Nov 1991 p 1498-1505
Publication Year: 1991
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: A 64-Mb CMOS dynamic RAM (DRAM) measuring 176.4 mm**2 has been fabricated using a 0.4- mu m N-substrate triple-well CMOS, double-poly, double-polycide, double-metal process technology. Asymmetrical stacked-trench capacitor (AST) cells, 0.9 mu m multiplied by 1.7 mu m each,

are laid out in a **PMOS** centered interdigitated twisted **bit-line** (PCITBL) scheme that achieves both low noise and high packing density. Three circuit techniques were developed to meet high-speed requirements. Using the preboosted **word-line** drive-line technique, a bypassed sense-amplifier drive-line scheme, and a quasi-static data transfer technique, a typical RAS access time of 33 ns and a typical column address access time of 15 ns have been achieved. 9 Refs.

34/3,AB/18 (Item 12 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02729019
E.I. Monthly No: EI8904032628
Title: 4-ns 4K multiplied by 1-bit two-port BiCMOS SRAM.
Author: Yang, Tsen-Shau; Horowitz, Mark A.; Wooley, Bruce A.
Corporate Source: Stanford Univ, Stanford, CA, USA
Source: IEEE Journal of Solid-State Circuits v 23 n 5 Oct 1988 p 1030-1040
Publication Year: 1988
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: The authors introduce a two-port BiCMOS static **random-access memory** (SRAM) cell that combines ECL-level **word-line** voltage swings and emitter-follower **bit-line** coupling with a static CMOS latch for data storage. With this cell, referred to as a CMOS storage emitter access (CSEA) cell, it is possible to achieve access times comparable to those of high-speed bipolar SRAMs while preserving the high density and low power of CMOS memory arrays. The memory can be read and written simultaneously and is therefore well-suited to applications such as high-speed caches and video memories. A read access time of 3.8 ns at a power dissipation of 520 mW has been achieved in an experimental 4K multiplied by 1-bit two-port memory integrated in a 1.5- mu m 5-GHz BiCMOS technology. The access time in this prototype design is nearly temperature-insensitive, increasing to only 4 ns at a case temperature of 100 degree C. 13 Refs.

34/3,AB/19 (Item 13 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02723208
E.I. Monthly No: EI8903020925
Title: 16 ns 256k multiplied by 1 CMOS SRAM.
Author: Flannagan, Stephen; Nogle, Scott; Faber, Allen; Herr, Norm; Mauntel, Rick; Engles, Bruce; Kung, Roger
Corporate Source: Motorola Memory Products Div, Austin, TX, USA
Conference Title: 1988 IEEE International Solid-State Circuits Conference - Digest of Technical Papers (31st ISSCC). First Edition.
Conference Location: San Francisco, CA, USA Conference Date: 19880217
E.I. Conference No.: 11868
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference. Publ by Lewis Winner, Coral Gables, FL, USA.. Available from IEEE Service Cent (cat n 88CH2562-7) Piscataway, NJ, USA. p 182-183, 360
Publication Year: 1988
CODEN: DTPCDE
Language: English
Abstract: A 256K multiplied by 1 SRAM (static **random-access**

memory) fabricated with a double-metal 1.2- mu m CMOS process is reported. Duplicated pads allow for multiple-package compatibility. The chip architecture uses sixteen subarray blocks to reduce power consumption, and local **word-lines** and **bit-lines** to assist in signal development. The address buffer design uses dual input stages to overcome the traditional difficulty of providing uniform dc margins in the presence of hysteresis. The active current is shown as a function of V//D//D// and as a function of cycle time. At 5 V, the active current is 48 mA at a 40 ns cycle (25 MHz).

34/3,AB/20 (Item 14 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02720814
E.I. Monthly No: EI8903020915
Title: 4 nsec 4K multiplied by 1 bit two-port BiCMOS SRAM.
Author: Yang, T. S.; Horowitz, M. A.; Wooley, B. A.
Corporate Source: Stanford Univ, CA, USA
Conference Title: Proceedings of the IEEE 1988 Custom Integrated Circuits Conference.
Conference Location: Rochester, NY, USA Conference Date: 19880516
E.I. Conference No.: 11798
Source: Proceedings of the Custom Integrated Circuits Conference. Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (cat n 88CH2584-1) Piscataway, NJ, USA. p 4.7/1-4
Publication Year: 1988
CODEN: PCICER
Language: English
Abstract: The authors introduce a two-port BiCMOS (bipolar complementary metal-oxide semiconductor) static memory cell that combines ECL (emitter-coupled-logic)-level **word-line** voltage swings and emitter-follower **bit line** coupling with a static CMOS latch to achieve access times comparable to those of high-speed bipolar SRAMs (static **random-access memories**), while preserving the high density and low power of CMOS memory arrays. The memory can be accessed for read and write independently and simultaneously, making it especially attractive for the design of video, cache, and other application-specific memories. An experimental 4K multiplied by 1 bit two-port memory integrated in a 1.5- mu m-5-GHz BiCMOS technology exhibits a read access time of 4 ns and a power dissipation of 550 mW. 4 Refs.

34/3,AB/21 (Item 15 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02518771
E.I. Monthly No: EI8802012209
Title: 25-NS 1-MBIT CMOS SRAM WITH LOADING-FREE **BIT LINES**.
Author: Matsui, Masataka; Ohtani, Takayuki; Tsujimoto, Jun-ichi; Iwai, Hiroshi; Suzuki, Azuma; Sato, Katsuhiko; Isobe, Mitsuo; Hashimoto, Kazuhiko ; Saitoh, Mitsuchika; Shibata, Hideki; Sasaki, Hisayo; Matsuno, Tadashi; Matsunaga, Jun-ichi; Iizuka, Tetsuya
Corporate Source: Toshiba Corp, Kawasaki, Jpn
Source: IEEE Journal of Solid-State Circuits v SC-22 n 5 Oct 1987 p 733-740
Publication Year: 1987
CODEN: IJSCBC ISSN: 0018-9200
Language: ENGLISH

Abstract: A 128K X 8-b CMOS SRAM is described which achieves a 25 ns access time, less than 40 mA active current at 10 MHz, and 2 MU A standby current. The novel **bit-line** circuitry (loading-free **bit line**), using two kinds of NMOSFETs with different threshold voltages, improves **bit-line** signal speed and integrity. The two-stage local amplification technique minimizes the data-line delay. The dynamic double-**word-line** scheme (DDWL) allows the cell array to be divided into 32 sections along the **word-line** direction without a huge increase in chip area. This allows the DDWL scheme to reduce the core-area delay time and operating power to about half that of other conventional structures. A double-metal 0. 8 MU m twin-tub CMOS technology has been developed to realize the 5. 6 X 9. 5 MU **2 cell size and the 6. 86 X 15. 37 mm**2 chip size. 10 refs.

34/3,AB/22 (Item 16 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02518758
E.I. Monthly No: EI8802012200
Title: 4-MBIT DRAM WITH FOLDED-**BIT-LINE** ADAPTIVE SIDEWALL-ISOLATED CAPACITOR (FASIC) CELL.
Author: Mashiko, Koichiro; Nagatomo, Masao; Arimoto, Kazutami; Matsuda, Yoshio; Furutani, Kiyohiro; Matsukawa, Takayuki; Yamada, Michihiro; Yoshihara, Tsutomu; Nakano, Takao
Corporate Source: Mitsubishi Electric Corp, Jpn
Source: IEEE Journal of Solid-State Circuits v SC-22 n 5 Oct 1987 p 643-650
Publication Year: 1987
CODEN: IJSCBC ISSN: 0018-9200
Language: ENGLISH
Abstract: A 5-V 4-Mb word X 1-b/1-Mb word X 4-b dynamic RAM with a static column mode and fast page mode has been built in a 0. 8 MU m twin-tub CMOS technology with single-metal, two-polycide, and single poly-Si interconnections. It uses an innovative folded-**bit-line** adaptive sidewall-isolated capacitor (FASIC) cell that measures 10. 9 MU m**2 and requires only a 2 MU m trench to obtain a storage capacitor of 50 fF with 10 nm SiO//2 equivalent dielectric film. A shared-**PMOS** sense-amplifier architecture used in this DRAM provides a low power consumption, small C//B-to-C//S capacitance ratio, and accurate reference level for the nonboosted **word-line** scheme with little area penalty. These concepts have allowed the DRAM to be housed in the industry standard 300 mil dual-in-line package with performances of 90 ns RAS access time and 30 ns column address access time. 21 refs.

34/3,AB/23 (Item 17 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02276801
E.I. Monthly No: EIM8710-065776
Title: 25NS 1 MB CMOS SRAM.
Author: Ohtani, Takayuki; Hashimoto, Kazuhiko; Matsui, Masataka; Tsujimoto, Jun-ichi; Iwai, Hiroshi; Saitoh, Mitsuchika; Shibata, Hideki; Sasaki, Hisayo; Isobe, Mitsuo; Matsunaga, Jun-ichi; Iizuka, Tetsuya
Corporate Source: Toshiba Corp, Kanagawa, Jpn
Conference Title: 1987 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, First Edition.
Conference Location: New York, NY, USA Conference Date: 19870225

E.I. Conference No.: 10107
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1987. Publ by Lewis Winner, Coral Gables, FL, USA. Available from IEEE Service Cent (Cat n 87CH2367-1), Piscataway, NJ, USA p 264-265, 420
Publication Year: 1987
CODEN: DTPCDE
Language: English
Abstract: Summary form only given. The development of a 1-Mb chip with a typical address access time of 25 ns and typical operating current of 15 mA is described. Desired performance has been realized by **bit-line** circuitry, a two-stage sense amplifier utilizing renewed double **word-line** structure, address transition detection techniques, and a 0. 8- MU m CMOS process with double-level polysilicon and double-level aluminum layers. 1 ref.

34/3,AB/24 (Item 18 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02276798
E.I. Monthly No: EIM8710-065773
Title: 35 NS 1 MB CMOS SRAM.
Author: Komatsu, Takaaki; Okazaki, Nobumichi; Nishihara, Toshiyuki; Kayama, Shigeki; Hoshi, Naoya; Aoyama, Jun-ichi; Shimada, Takashi
Corporate Source: Sony Corp, Kanagawa, Jpn
Conference Title: 1987 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, First Edition.
Conference Location: New York, NY, USA Conference Date: 19870225
E.I. Conference No.: 10107
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1987. Publ by Lewis Winner, Coral Gables, FL, USA. Available from IEEE Service Cent (Cat n 87CH2367-1), Piscataway, NJ, USA p 258-259, 417
Publication Year: 1987
CODEN: DTPCDE
Language: English
Abstract: The RAM described is usable at TTL I/O levels and exhibits improved noise immunity. The RAM utilizes a divided **word line** with a memory cell array divided into 16 sections. Each section includes 1024 PLUS 8 rows, or columns, 8 I/Os and 8 sense amplifiers. Only 8 pairs of short data lines are connected to one sense amplifier. This architecture expedites sensing of the information on the selected **bit lines**. A zero V//t//h **NMOS** is used to balance the **bit line** voltages. As a result, the equalizing period is reduced to half that of a conventional **PMOS** scheme in the write recovery mode. The RAM was fabricated with double-polysilicon, double-aluminum CMOS technology, using 1. 0- MU m design rules. The memory cell measures 6. 4- MU m X 11. 6- MU m. 3 refs.

34/3,AB/25 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08850785 Genuine Article#: 335ZH Number of References: 15
Title: Plasma enhanced chemical vapor deposition Si-rich silicon oxynitride films for advanced self-aligned contact oxide etching in sub-0.25 mu m ultralarge scale integration technology and beyond (ABSTRACT AVAILABLE)

01/22/2003

Author(s): Kim JH (REPRINT) ; Yu JS; Ku JC; Ryu CK; Oh SJ; Kim SB; Kim JW; Hwang JM; Lee SY; Kouichiro I
Corporate Source: HYUNDAI ELECT IND CO LTD,SEMICOND ADV RES DIV, SAN 136-1/INCHON 467701/KYONGKI/SOUTH KOREA/ (REPRINT); TEL KOREA LTD,/YONGIN 449840/KYOUNGKI/SOUTH KOREA/; TOKYO ELECTRON YAMANASHI LTD,/YAMANASHI 407//JAPAN/
Journal: JOURNAL OF VACUUM SCIENCE & TECHNOLOGY A-VACUUM SURFACES AND FILMS , 2000, V18, N4,1 (JUL-AUG), P1401-1410
ISSN: 0734-2101 Publication date: 20000700
Publisher: AMER INST PHYSICS, 2 HUNTINGTON QUADRANGLE, STE 1NO1, MELVILLE, NY 11747-4501
Language: English Document Type: ARTICLE
Abstract: We intentionally introduced excessive Si during the SiOxNy film deposition in order to increase the etch selectivity-to-SiOxNy for advanced self-aligned contact (SAC) etching in sub-0.25 mu m ultralarge scale integration devices. The SiOxNy layer was deposited at a conventional plasma enhanced chemical vapor deposition chamber by using a mixture of SiH4, NH3, N2O, and He. The gas mixing ratio was optimized to get the best etch selectivity and low leakage current. The best result was obtained at 10% Si-SiOxNy. In order to employ SiOxNy film as an insulator as well as a SAC barrier, the leakage current of SiOxNy film was evaluated so that SiOxNy may have the low leakage current characteristics. The leakage current of 10% Si-SiOxNy film was 7 x 10(-9) A/cm(2). Besides, the Si-rich SiOxNy layer excellently played the roles of antireflection coating for **word line** and **bit line** photoresist patterning and sidewall spacer to build a **metal-oxide-semiconductor transistor** as well as a SAC oxide etch barrier. The contact oxide etching with the Si-rich SiOxNy film was done using C4F8/CH2F2/Ar in a dipole ring magnet plasma. As the C4F8 flow rate increases, the oxide etching selectivity-to-SiOxNy increases but etch stop tends to happen. Our optimized contact oxide etch process showed the high selectivity to SiOxNy larger than 25 and a wide process window (greater than or equal to 5 sccm) for the C4F8 flow rate. When the Si-rich SiOxNy SAC process was applied to a gigabit **dynamic random access memory** of cell array, there was no electrical short failure between conductive layers. (C) 2000 American Vacuum Society. [S0734-2101(00) 16504-2].

34/3,AB/26 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

14481979 PASCAL No.: 00-0143646
Innovating SRAM design and test program for fast process related defect recognition and failure analysis
In-line methods and monitors for process and yield improvement : Santa Clara CA, 22-23 September 1999
COPPENS P; VANHOREBEEK G; DE BACKER E; YUAN X J
AJURIA Sergio, ed; JAKUBCZAK Jerome F, ed
Alcatel Microelectronics, Oudenaarde, Belgium; IMEC, Leuven, Belgium
International Society for Optical Engineering, Bellingham WA, United States.
In-line methods and monitors for process and yield improvement. Conference (Santa Clara CA USA) 1999-09-22
Journal: SPIE proceedings series, 1999, 3884 290-297
Language: English
A special SRAM has been designed as a yield enhancement vehicle in a 0.35 mu m CMOS technology. Extra design rules were added to encourage process defects on certain places and discourage them on others. From the failure

signature of a memory cell (0 or I failure) and its failure extent (single cell, double cell, **bitline**, **wordline** ,) one can uniquely determine the process related cause of the failure. A dedicated test program has been developed to find the most common failures in a memory cell (e.g. floating **bitline**, **bitline** shorted to ground or Vdd, shorts between the nodes of the cell,). The innovating characteristics of the design allow to link these failures in an SRAM with high probability to a process related defect and its location within the memory cell. By simply testing the SRAM the main cause of failure can be found which can help to drive yield improvement, without doing intensive failure analysis. In this paper the design philosophy and the test methodology of this SRAM are described, illustrated with some examples of process related defects that proved the usefulness and the strength of the design and the test program.

34/3,AB/27 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

11554885 PASCAL No.: 94-0437802
Superconductor-semiconductor memories
III. Electronics
GHOSHAL U; KROGER H; VAN DUZER T
GREEN Michael A, ed
Univ. California, electronics res. lab., dep. electrical eng. computer sci., Berkeley CA 94720, USA
Lawrence Berkeley Laboratory, Berkeley CA 94720, USA
Applied Superconductivity Conference, Terra incognita.
ASC'92. Conference (Chicago IL USA) 1992-08-23
Journal: IEEE Transactions on applied superconductivity, 1993, 3 (1 p.4) 2315-2318
Language: English
We describe new types of hybrid superconductor-semiconductor RAMs which utilize the current switches in superconductive electronics to remove important constraints on the design of semiconductor memories and achieve performances unattainable by the individual technologies separately. We focus on a voltage **word line** RAM architecture and illustrate the basic designs in terms of a low-T SUB c Josephson-CMOS technology which we are currently developing at UC Berkeley SUP 1 . We discuss the design of interface circuits, **word-line** drivers, memory cells, and fluxoelectronic current sensing of **bit lines** . Current projections for 4 K operation indicate that sub-nanosecond 64 kb RAMs using a 0.8 mu m CMOS technology

34/3,AB/28 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

11403025 PASCAL No.: 94-0233409
A 5.8-ns 256-kb BiCMOS TTL SRAM with T-shaped **bit line** architecture
SHIOMI T; WADA T; OHBAYASHI S; OHBA A; HONDA H; ISHIGAKI Y; HINE S; ANAMI K; SUZUKI K; SUMI T
Mitsubishi Electric Corp., Itami, Japan
Journal: IEEE journal of solid-state circuits, 1993, 28 (12) 1362-1369
Language: English
This paper presents a new **bit line** architecture named T-shaped **bit line** architecture (TSBA), which is suitable for

high speed, high density, and/or large bit-wide configuration SRAM's. TSBA, utilizing orthogonal complimentary **bit lines** in parallel with the **word lines**, is the solution to **bit line** pitch constraint for direct bipolar column sensing. This TSBA is applied to a 256-Kb SRAM with a typical access time of 5.8 ns. To achieve access times below 6 ns, this SRAM employs a bipolar Darlington column sense amplifier, a hierarchical column decoding scheme, a data bus shielding layout combined with TSBA, and a 0.8- mu m BiCMOS technology

34/3,AB/29 (Item 4 from file: 144)
DIALOG(R)File 144:Pascal

10637896 PASCAL No.: 93-0147174
A 15-ns 16-Mb CMOS SRAM with interdigitated **bit-line** architecture : Memory and logic
MATSUMIYA M; KAWASHIMA S; SAKATA M; OOKURA M; MIYABO T; KOGA T; ITABASHI K; MIZUTANI K; SHIMADA H; SUZUKI N
Fujitsu Ltd, Nakahara-ku Kawasaki 211, Japan
Journal: IEEE journal of solid-state circuits, 1992, 27 (11) 1497-1503
Language: English
This paper describes circuit techniques for a reduced-voltage-amplitude data bus, fast access 16-Mb CMOS SRAM. An interdigitated **bit-line** architecture reduces data bus line length, thus minimizing bus capacitance. A hierarchical sense amplifier consists of 32 local sense amplifiers and a current sense amplifier. The current sense amplifier is used to reduce the data bus voltage amplitude and the sensing of the 16-b data bus signals in parallel. With these techniques we achieved a fast access time of 15 ns and a small active power of 165 mW in a 16-Mb CMOS SRAM. A split-**word-line** layout memory cell, with double-gate **pMOS** thin-film transistors (TFT's), keeps the transistor width stable while providing high-stability memory cell characteristics

34/3,AB/30 (Item 5 from file: 144)
DIALOG(R)File 144:Pascal

10126303 PASCAL No.: 92-0332056
A 1-V operating 256-kb full-CMOS SRAM
SEKIYAMA A; SEKI T; NAGAI S; IWASE A; SUZUKI N; HAYASAKA M
Fujitsu VLSI Ltd, MOS LSI design div., Kasugai 487, Japan
Journal: IEEE journal of solid-state circuits, 1992, 27 (5) 776-782
Language: English
A I-V operating 256-kb full-CMOS SRAM to be used in 1.5-V battery-based applications is presented. A reference **word line** and address transition detection (ATD) are used as timing control techniques to achieve adjustable timing of critical signals with a 1.5-V battery. The key circuit of the pulse sequence block is the ATD pulse generator circuit. We use a newly modified Schmitt trigger delay circuit. To reduce supply line noise in the chip, we needed to lower the peak of **bit-line** charge-up current. This was done by applying a divided **word-line** technique and a newly adopted staggered **bit-line** equalizing pulse technique

34/3,AB/31 (Item 6 from file: 144)
DIALOG(R)File 144:Pascal

01/22/2003

10075345 PASCAL No.: 92-0280849
A pulsed sensing scheme with a limited **bit-line** swing
SCHEUERLEIN R E; KATAYAMA Y; KIRIHATA T; SAKAUE Y; SATOH A; SUNAGA T; YOSHIKAWA T; KITAMURA K; DHONG S H
IBM Japan, IBM res. lab., Chiyoda-ku Tokyo 102, Japan
Journal: IEEE journal of solid-state circuits, 1992, 27 (4) 678-682
Language: English
This paper presents a pulsed sensing scheme with a limited **bit-line** swing designed for 4-Mb CMOS high-speed DRAM's (HSDRAM's) and beyond. It uses a standard CMOS cross-coupled sense amplifier and limites the swing by means of a pulsed sense clock. The signal loss that would occur if the **bitline** swing was not exactly limited to one threshold above the **word-line** 's low level is avoided by using a small reference voltage generator and trench decoupling capacitors. The new sensing scheme was successfully implemented on an experimental HSDRAM fabricated by using 0.7- mu m L SUB e SUB f SUB f CMOS technology, and thus a high-speed random access time of 15 ns and a low power dissipation of 144 mW were obtained for 512-kb array activation with a fast cycle time of 60 ns at 3.6 V

34/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6747707 INSPEC Abstract Number: B2000-12-1265D-017, C2000-12-5320G-004
Title: Process integration trends for embedded DRAM
Author(s): Takato, H.; Koike, H.; Yoshida, T.; Ishiuchi, H.
Author Affiliation: Microelectron. Eng. Lab., Toshiba Corp., Yokohama, Japan
Conference Title: ULSI Process Integration. Proceedings of the First International Symposium (Electrochemical Society Proceedings Vol.99-18) p.107-19
Editor(s): Claeys, C.L.; Iwai, H.; Bronner, G.; Fair, R.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1999 Country of Publication: USA xiii+386 pp.
ISBN: 1 56677 241 9 Material Identity Number: XX-2000-00269
Conference Title: Proceedings of ULSI Process Integration
Conference Sponsor: Electrochem. Soc
Conference Date: 17-22 Oct. 1999 Conference Location: Honolulu, HI, USA
Language: English
Abstract: Issues and development trends with respect to embedded DRAM (**eDRAM**) technology are reviewed by referring to real implementations for 0.5 mu m, 0.35 mu m and 0.25 mu m generations. Chip performance has been progressively improved throughout the development of 0.5 mu m, 0.35 mu m and 0.25 mu m **eDRAM** . However, the number of process steps has increased compared to that for commodity DRAM. To avoid this problem and achieve the highest possible device performance, future directions for embedded DRAM technologies, including **MOSFET** structure, memory cells, process cost and performance, are also discussed. For the **MOSFET** structure, the logic-based **MOSFET** process offers more advantages than the DRAM-based one for future **eDRAM** generations. For memory cell structure, the trench cell is expected to be more useful for future **eDRAM** compared to the stacked cell. In order to combine the trench cell and logic based **MOSFET** process, a new embedded DRAM technology is proposed. This process technology provides full process compatibility with high performance logic and a minimum number of process steps, resulting in low process cost and short TAT (turnaround time). A DRAM array macro has been fabricated using this technology with Co salicide, dual work function gate and aluminum **bit-line** processes, and excellent DRAM retention characteristics have been confirmed using a negative **word-line** bias scheme.
Subfile: B C

34/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6737400 INSPEC Abstract Number: B2000-12-0520F-010
Title: Plasma enhanced chemical vapor deposition Si-rich silicon oxynitride films for advanced self-aligned contact oxide etching in sub-0.25 mu m ultralarge scale integration technology and beyond
Author(s): Jeong-Ho Kim; Jae-Seon Yu; Ja-Chun Ku; Choon-Kun Ryu; Su-Jin Oh; Si-Bum Kim; Jin-Woong Kim; Jeong-Mo Hwang; Su-Youb Lee; Kouichiro, I.
Author Affiliation: Semicond. Adv. Res. Div., Hyundai Electron. Ind. Co. Ltd., South Korea
Journal: Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films) Conference Title: J. Vac. Sci. Technol. A, Vac. Surf. Films (USA)

01/22/2003

vol.18, no.4, pt.1-2 p.1401-10
Publisher: AIP for American Vacuum Soc,
Publication Date: July-Aug. 2000 Country of Publication: USA
CODEN: JVTAD6 ISSN: 0734-2101
SICI: 0734-2101(200007/08)18:4:1/2L.1401:PECV;1-2
Material Identity Number: D746-2000-005
U.S. Copyright Clearance Center Code: 0734-2101/2000/18(4)/1401(10)/$15.00
Conference Title: 46th National Symposium of the American Vacuum Society. Vacuum, Surfaces, and Films
Conference Date: 25-29 Oct. 1999 Conference Location: Seattle, WA, USA
Language: English
Abstract: We intentionally introduced excessive Si during the SiO/sub x/N/sub y/ film deposition in order to increase the etch selectivity-to-SiO/sub x/N/sub y/ for advanced self-aligned contact (SAC) etching in sub-0.25 mu m ultralarge scale integration devices. The SiO/sub x/N/sub y/ layer was deposited at a conventional plasma enhanced chemical vapor deposition chamber by using a mixture of SiH/sub 4/, NH/sub 3/, N/sub 2/O, and He. The gas mixing ratio was optimized to get the best etch selectivity and low leakage current. The best result was obtained at 10% Si-SiO/sub x/N/sub y/. In order to employ SiO/sub x/N/sub y/ film as an insulator as well as a SAC barrier, the leakage current of SiO/sub x/N/sub y/ film was evaluated so that SiO/sub x/N/sub y/ may have the low leakage current characteristics. The leakage current of 10% Si-SiO/sub x/N/sub y/ film was 7*10/sup -9/ A/cm/sup 2/. Besides, the Si-rich SiO/sub x/N/sub y/ layer excellently played the roles of antireflection coating for **word line** and **bit line** photoresist patterning and sidewall spacer to build a **metal-oxide-semiconductor transistor** as well as a SAC oxide etch barrier. The contact oxide etching with the Si-rich SiO/sub x/N/sub y/ film was done using C/sub 4/F/sub 8//CH/sub 2/F/sub 2//Ar in a dipole ring magnet plasma. As the C/sub 4/F/sub 8/ flow rate increases, the oxide etching selectivity-to-SiO/sub x/N/sub y/ increases but etch stop tends to happen. Our optimized contact oxide etch process showed the high selectivity to SiO/sub x/N/sub y/ larger than 25 and a wide process window (>or=5 sccm) for the C/sub 4/F/sub 8/ flow rate. When the Si-rich SiO/sub x/N/sub y/ SAC process was applied to a gigabit **dynamic random access memory** of cell array, there was no electrical short failure between conductive layers.
Subfile: B

34/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

03854525 INSPEC Abstract Number: B91023599
Title: Buried **bit-line** cell for 64 Mb DRAMs
Author(s): Kohyama, Y.; Yamamoto, T.; Sudo, A.; Watanabe, T.; Tanaka, T.
Author Affiliation: Toshiba Corp., Kawasaki, Japan
Conference Title: 1990 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.90CH2874-6) p.17-18
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA xvii+143 pp.
U.S. Copyright Clearance Center Code: CH2874-6/90/0000-0017$01.00
Conference Sponsor: IEEE; Japan Soc. Appl. Phys
Conference Date: 4-7 June 1990 Conference Location: Honolulu, HI, USA
Language: English
Abstract: The authors propose a buried **bit-line** (BBL) stacked capacitor cell structure for high-density **dynamic random**

access memories (DRAMs). The cell area can be reduced to as small as 8.7F/sup 2/, where F is the lithographic feature size. A 2.25- mu m/sup 2/ cell area is achieved using a 0.51- mu m feature size. A 1.4- mu m/sup 2/ cell area is attainable using a 0.4- mu m feature size. The memory-cell vertical size (2F) includes a line and space for a trench isolation pattern in which the buried **bit-line** is formed. The horizontal size (4F+a) includes two **word-line** line and space pairs and a **word-line** to **bit-line** contact alignment tolerance denoted by a. A storage node contact is self-aligned to the **word-line** . Since the a is considered to be less than F/2, a cell area of less than 9F/sup 2/ is realized. If the **bit-line** contact is also self-aligned to the **word-line**, an 8F/sup 2/ cell area can in theory be realized.
Subfile: B

34/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

01511422 INSPEC Abstract Number: B80024087
Title: Fabrication of V-**MOS** or U-**MOS random-access memory** cells with a self-aligned **word line**
Author(s): Chang, T.S.; Ogura, S.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.22, no.7 p.2768-71
Publication Date: Dec. 1979 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: A self-aligned **word line** for V-**MOS** and U-**MOS random-access memories** reduces the cell areas, **bit line** capacitance and **word line** resistance.
Subfile: B

34/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

01422567 INSPEC Abstract Number: B79047285, C79030068
Title: One-device cells for **dynamic random-access memories**: a tutorial
Author(s): Rideout, V.L.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Journal: IEEE Transactions on Electron Devices vol.ED26, no.6 p. 839-52
Publication Date: June 1979 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
Language: English
Abstract: The evolutionary development of one-device cells for **dynamic random-access memory** (RAM) integrated circuits is described. From an examination of the areal layout (planar top view) and the cross section (vertical topography), various memory cells are compared in a systematic manner. Structural features such as contact via formation, **bit-line** and **word-line** pitch, metal step coverage, and cell placement along the **bit line** are also considered. Some new dynamic RAM cell concepts such as doubly doped storage capacitors, self-registering contacts, and **VMOS** FET's are discussed. From an examination of commercially available dynamic RAM chips, a basic lithographic groundrule was determined.

01/22/2003

Subfile: B C

34/3,AB/6 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1192950 NTIS Accession Number: PB85-226090
One-M bit **NMOS** Dynamic RAM
Sakui, K. ; Miyawaki, N. ; Nakayama, R.
Toshiba Corp., Tokyo (Japan).
Corp. Source Codes: 021559000
c1985 4p
Languages: Japanese
Journal Announcement: GRAI8521
Text in Japanese.
Included in Toshiba Review, v40 n6 p478-481 1985.
NTIS Prices: (Order as PB85-226074, PC E05/MF E01)
The high performance 1-M words x 1-bit **NMOS** dynamic RAM has been developed by using proprietary BOX (buried oxide) isolation and two-level aluminum metalization techniques. The memory cell, adopting a novel folded capacitor cell structure realizing a large cell capacitance (70 fF), enables the RAM to operate with large noise margin and high alpha particle immunity. In order to realize high-speed and low-power operation, the RAM utilises the reduction of **word line** resistance (by means of second-level Al interconnection), high-speed sense amplifier system, partial activation scheme of memory cell arrays, and reduction of **bit -line** length. It has achieved 30 ns of CAS access time and 270 mW of active power dissipation at 260 ns cycle time.

34/3,AB/7 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06057013
E.I. No: EIP02216955097
Title: A capacitor-less 1T-DRAM cell
Author: Okhonin, S.; Nagoga, M.; Sallese, J.M.; Fazan, P.
Corporate Source: LEG Swiss Federal Inst. of Technol., CH-1015 Lausanne, Switzerland
Source: IEEE Electron Device Letters v 23 n 2 February 2002. p 85-87
Publication Year: 2002
CODEN: EDLEDZ ISSN: 0741-3106
Language: English
Abstract: A simple true 1 transistor **dynamic random access memory** (DRAM) cell concept is proposed for the first time, using the body charging of partially-depleted SOI devices to store the logic "1" or "0" binary states. This cell is two times smaller in area than the conventional 8F**2 1T/1C DRAM cell and the process of its manufacturing does not require the storage capacitor fabrication steps. This concept will allow the manufacture of simple low cost DRAM and embedded DRAM chips for 100 and sub-100 nm generations. 12 Refs.

34/3,AB/8 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05587584
E.I. No: EIP00065217411

01/22/2003

Title: Robust 8F**2 ferroelectric RAM cell with depletion device (DeFeRAM)
Author: Braun, Georg; Hoenigschmid, Heinz; Schlager, Tobias; Weber, Werner
Corporate Source: Infineon Technologies AG, Munich, Ger
Conference Title: The 1999 Symposium on VLSI Circuits
Conference Location: Kyoto, Jpn Conference Date: 20990617-20990619
E.I. Conference No.: 56947
Source: IEEE Journal of Solid-State Circuits v 35 n 5 2000. p 691-696
Publication Year: 2000
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: This paper describes an area-penalty-free, leakage-compensated, and noise-immune 8F**2 cell design suitable for high-density, low-power ferroelectric RAM (FeRAM) generations. The new concept features a 1T1C ferroelectric memory cell containing an additional depletion device (DeFeRAM) controlled by the passing **word line** in a folded **bit-line** architecture. The depletion device permits the use of a common cell plate at intermediate voltage level. A highly reliable three-level **word-line** driver circuit design is discussed. (Author abstract) 7 Refs.

34/3,AB/9 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05583444
E.I. No: EIP00065217433
Title: 0.5- mu m, 3-V, 1T1C, 1-Mbit FRAM with a variable reference **bit-line** voltage scheme using a fatigue-free reference capacitor
Author: Ogiwara, Ryu; Tanaka, Sumio; Itoh, Yasuo; Miyakawa, Tadashi; Takeuchi, Yoshiaki; Doumae, Sumiko Mano; Takenaka, Hiroyuki; Kunishima, Iwao; Shuto, Susumu; Hidaka, Osamu; Ohtsuki, Sumito; Tanaka, Shin-ichi
Corporate Source: Toshiba Corp, Yokohama, Jpn
Source: IEEE Journal of Solid-State Circuits v 35 n 4 2000. p 545-551
Publication Year: 2000
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: A 0.5- mu m, 3-V operated, 1T1C, 1-Mbit FRAM with 160-ns access time has been developed. In FRAM, a reference voltage design using a ferroelectric capacitor is difficult because of the degradation due to fatigue, a chip-to-chip variation, and a temperature dependence. A variable reference voltage scheme is generated to solve this problem, boosting a fatigue-free and temperature-independent **MOS** reference capacitance by a driver. The driver is operated from a compact reference voltage generator that provides 32 equally divided voltages and occupies only half the layout area of a conventional one. During sense operation, memory-cell capacitance C//f//e//r//r is larger than reference-cell capacitance C//M//O//S. A double **word-line** pulse scheme has also been developed to eliminate a **bit-line** capacitance imbalance in the **bit-line** pairs, where a memory cell and a reference cell are separated from the **bit-line** pairs during sense operation. A six-order improvement in imprint lifetime has been achieved by the new scheme. (Author abstract) 5 Refs.

34/3,AB/10 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05050777
E.I. No: EIP98074264245
Title: 3.6 mW 1.4 V SRAM with non-boosted, vertical bipolar **bitline** contact memory cell
Author: Sato, H.; Nagaoka, H.; Honda, H.; Maki, Y.; Wada, T.; Arita, Y.; Tsutsumi, K.; Yamada, M.
Corporate Source: Mitsubishi Electric Corp, Hyogo, Jpn
Conference Title: Proceedings of the 1998 IEEE 45th International Solid-State Circuits Conference, ISSCC
Conference Location: San Francisco, CA, USA Conference Date: 19980205-19980207
E.I. Conference No.: 48558
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1998. IEEE, Piscataway, NJ, USA,98CH36156. p 352-353, 463 PAPER SP 22.3
Publication Year: 1998
CODEN: DTPCDE ISSN: 0193-6530
Language: English
Abstract: Low-voltage static **random access memory** (SRAM) operating at less than 3 V are used for handy terminals, however, demand for lower-voltage operation has increased. It is difficult to reduce operating voltage below 2.5 V with the conventional low-power SRAM with 4 **nMOS**-transistor cell. Although a full CMOS cell or a boosted **word line** technique can reduce operating voltage, they have certain problems. A 256 kb, low-power SRAM using a bipolar **bit line** contact (BBC) memory cell used to solve these problems which features small cell, low-operating voltage, low power distribution and fast access is presented. 2 Refs.

34/3,AB/11 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04970705
E.I. No: EIP98034104375
Title: Low temperature metal-based cell integration technology for gigabit and embedded DRAMs
Author: Yoshida, Makoto; Kumauchi, Takahiro; Kawakita, Keizo; Ohashi, Naofumi; Enomoto, Hiroyuki; Umezawa, Tadashi; Yamamoto, Naoki; Asano, Isamu ; Tadaki, Yoshitaka
Corporate Source: Hitachi Ltd, Tokyo, Jpn
Conference Title: Proceedings of the 1997 International Electron Devices Meeting
Conference Location: Washington, DC, USA Conference Date: 19971207-19971210
E.I. Conference No.: 48095
Source: Proceedings of the IEEE Hong Kong Electron Devices Meeting 1997. IEEE, Piscataway, NJ, USA,97CH36103. p 41-44
Publication Year: 1997
CODEN: 002525
Language: English
Abstract: An advanced memory cell structure with poly/metal **word lines** and metal **bit lines** is proposed. The thermal processes are carefully designed for the metal-based cell to be consistent with narrow gap filling, wet cleaning, planarity, and the contact process. The extremely low temperature process also helps suppress the short channel effect of the **MOS** transistors. The fully self-aligned contact and via-hole technology provides the minimum memory cell area. This technology is promising for future gigabit DRAMs and embedded DRAMs. (Author abstract)

6 Refs.

34/3,AB/12 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04624882
E.I. No: EIP97023516176
Title: 0.23 mu m**2 double self-aligned contact cell for gigabit DRAMs with a Ge-added vertical epitaxial Si pad
Author: Koga, H.; Kasai, N.; Hada, H.; Tatsumi, T.; Mori, H.; Iwao, S.; Saino, K.; Yamaguchi, H.; Nakajima, K.; Yamada, Y.; Tokunaga, K.; Hirasawa, S.; Yoshida, K.; Nishizawa, A.; Hashimoto, T.; et al
Corporate Source: NEC Corp, Kanagawa, Jpn
Conference Title: Proceedings of the 1996 IEEE International Electron Devices Meeting
Conference Location: San Francisco, CA, USA Conference Date: 19961208-19961211
E.I. Conference No.: 46059
Source: Technical Digest - International Electron Devices Meeting 1996. IEEE, Piscataway, NJ, USA,96CH35961. p 589-592
Publication Year: 1996
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: A new stacked capacitor memory cell with folded **bit-line** arrangement has been developed using a double self-aligned contact technology. By using a combination of a vertical epitaxial growth Si pad and Si//3N//4 caps as etch stop layers on both the **bit-lines** and **word-lines**, the cell area using 0.15 mu m design rule can be reduced to 0.23 mu m**2 with 0.1 mu m alignment tolerance. Through addition of germanium (Ge) to the Si pad, the controllability of epitaxially grown Si pad features can be improved, resulting in an increase in the growth rate ratio of perpendicular to lateral directions by a factor of 4 and a decrease in resistance of the epi pad from 5k Omega to 1k Omega . (Author abstract) 6 Refs.

34/3,AB/13 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04313529
E.I. No: EIP95122958382
Title: Current direction sense technique for multi-port SRAMs
Author: Izumikawa, Masanori; Yamashina, Masakazu
Corporate Source: NEC Corp, Kanagawa, Jpn
Conference Title: Proceedings of the 1995 Symposium on VLSI Circuits
Conference Location: Kyoto, Jpn Conference Date: 19950608-19950610
E.I. Conference No.: 44078
Source: IEEE Symposium on VLSI Circuits, Digest of Technical Papers 1995. IEEE, Piscataway, NJ, USA,95CH35780. p 23-24
Publication Year: 1995
CODEN: 85PXA5
Language: English
Abstract: Single-end sense amplifiers which do not require a reference voltage would be most desirable for multi-port SRAMs. This paper describes a current-direction sense circuit which transforms current direction into a logic value. It operates four times faster than a CMOS inverter, and with it, it is possible to produce single-end 200 MHz 64 kb SRAMs whose total power consumption is nearly as low as that required for the memory cell

currents alone in conventional SRAMs. Also presented is a write **bit-line** and **word-line** swing. When this circuit is applied to be used in a 200 MHz 64 kb SRAM, it is possible to reduce by one-third the power consumption required for **bit-line** driving and pseudo-read cell current (0.25 mu m CMOS). 1 Refs.

34/3,AB/14 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04001605
E.I. No: EIP94122451194
Title: Vertical Phi -shape transistor (V Phi T) cell for 1Gbit DRAM and beyond
Author: Maeda, S.; Maegawa, S.; Ipposhi, T.; Nishimura, H.; Kuriyama, H.; Tanina, O.; Inoue, Y.; Nishimura, T.; Tsubouchi, N.
Corporate Source: ULSI Lab Mitsubishi Electric Corp, Hyogo, Jpn
Conference Title: Proceedings of the 1994 Symposium on VLSI Technology
Conference Location: Honolulu, HI, USA Conference Date: 19940607-19940609
E.I. Conference No.: 21361
Source: Digest of Technical Papers - Symposium on VLSI Technology 1994. IEEE, Piscataway, NJ, USA,94CH3433-0. p 133-134
Publication Year: 1994
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: We propose a Vertical Phi -shape Transistor (V Phi T) cell for 1Gbit DRAM and beyond. The V Phi T is a vertical **MOSFET** whose gate surrounds its channel region like a Greek alphabet Phi . It is built by penetration of the gate electrode (equals **word line**) which has been formed beforehand. Application of the V Phi T for DRAM cell brings about cell size reduction to 50% and process simplification of about 10% at least, mainly because its **bit line** contact and the V Phi T are vertically aligned and storage node contact is eliminated. We have indicated that the V Phi T is an interesting candidate for the gigabit DRAM in view of size, cost and performance. (Author abstract) 12 Refs.

34/3,AB/15 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03894125
E.I. No: EIP94071336921
Title: Design rule relaxation approach for high-density DRAMs
Author: Saeki, Takanori; Kakehashi, Eiichiro; Mori, Hidemitu; Koga, Hiroki; Noda, Kenji; Fujita, Mamoru; Sugawara, Hiroshi; Nagata, Kyoichi; Nishimoto, Shozo; Murotani, Tatsunori
Corporate Source: NEC Corp, Sagamihara-shi, Jpn
Source: IEICE Transactions on Electronics v E77-C n 3 Mar 1994. p 406-415
Publication Year: 1994
CODEN: IELEEJ ISSN: 0916-8524
Language: English
Abstract: A design rule relaxation approach is one of the most important requirements for high density DRAMs. The approach relaxes the design rule of a element in comparison with the memory cell size and provides high density DRAMs with the minimum development of a scaled-down **MOS** structure and a fine patterning lithography process. This paper describes two design rule relaxation approaches, a close-packed folded (CPF) **bit-line** cell array layout and a Boosted Dual **Word-**

Line scheme. The CPF cell array provides 1.26 times wider active area pitch and maximum 1.5 times wider isolation width. The Boosted Dual **Word-Line** scheme provides 2**n times wider 1st Al pitch on memory cell array, double **word-line** driver pitch and 1.5 times larger design rule for 1st Al and contacts under 1st Al. Especially wide design rule of the Boosted Dual **Word-Line** scheme provides several times depth of focus (DOF) for 1st Al wiring which gives several times higher storage node and larger capacitance for capacitor over **bit-line** (COB) stacked capacitor cells. These approaches are successfully implemented in a 4 Mb DRAM test chip with a 0.9 multiplied by 1.8 mu m**2 memory cell. (Author abstract) 14 Refs.

34/3,AB/16 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03783613
E.I. No: EIP94011186903
Title: Single-**bit-line** cross-point cell activation (SCPA) architecture for ultra-low-power SRAM's
Author: Ukita, Motomu; Murakami, Shuji; Yamagata, Tadato; Kurijama, Hirotada; Nishimura, Yasumasa; Anami, Kenji
Corporate Source: Mitsubishi Electric Corp, Itami City, Jpn
Source: IEEE Journal of Solid-State Circuits v 28 n 11 Nov 1993. p 1114-1118
Publication Year: 1993
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: This paper describes a single-**bit-line** cross-point cell activation (SCPA) architecture, which has been developed to reduce active power consumption and to avoid increase in the size of high-density SRAM chips, such as 16-Mb SRAM's and beyond. A new **PMOS** precharging boost circuit, introduced to realize the single-**bit-line** structure, is also discussed. This circuit is suitable for operation under low-voltage power supply conditions. The SCPA architecture with the new **word-line** boost circuit is demonstrated with the experimental device, which is fabricated by 0.4- mu m CMOS wafer process technology. (Author abstract) 3 Refs.

34/3,AB/17 (Item 11 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03394565
E.I. Monthly No: EI9203031448
Title: A 33-ns 64-Mb DRAM.
Author: Oowaki, Yukihito; Tsuchida, Kenji; Watanabe, Yohji; Takashima, Daisaburo; Ohta, Masako; Nakano, Hiroaki; Watanabe, Shigeyoshi; Nitayama, Akihiro; Horiguchi, Fumio; Ohuchi, Kazunori; Masuoka, Fujio
Corporate Source: Toshiba Corp, Saiwai-ku, Kawasaki, Japan
Source: IEEE Journal of Solid-State Circuits v 26 n 11 Nov 1991 p 1498-1505
Publication Year: 1991
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: A 64-Mb CMOS dynamic RAM (DRAM) measuring 176.4 mm**2 has been fabricated using a 0.4- mu m N-substrate triple-well CMOS, double-poly, double-polycide, double-metal process technology. Asymmetrical stacked-trench capacitor (AST) cells, 0.9 mu m multiplied by 1.7 mu m each,

are laid out in a **PMOS** centered interdigitated twisted **bit-line** (PCITBL) scheme that achieves both low noise and high packing density. Three circuit techniques were developed to meet high-speed requirements. Using the preboosted **word-line** drive-line technique, a bypassed sense-amplifier drive-line scheme, and a quasi-static data transfer technique, a typical RAS access time of 33 ns and a typical column address access time of 15 ns have been achieved. 9 Refs.

34/3,AB/18 (Item 12 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02729019
E.I. Monthly No: EI8904032628
Title: 4-ns 4K multiplied by 1-bit two-port BiCMOS SRAM.
Author: Yang, Tsen-Shau; Horowitz, Mark A.; Wooley, Bruce A.
Corporate Source: Stanford Univ, Stanford, CA, USA
Source: IEEE Journal of Solid-State Circuits v 23 n 5 Oct 1988 p 1030-1040
Publication Year: 1988
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: The authors introduce a two-port BiCMOS static **random-access memory** (SRAM) cell that combines ECL-level **word-line** voltage swings and emitter-follower **bit-line** coupling with a static CMOS latch for data storage. With this cell, referred to as a CMOS storage emitter access (CSEA) cell, it is possible to achieve access times comparable to those of high-speed bipolar SRAMs while preserving the high density and low power of CMOS memory arrays. The memory can be read and written simultaneously and is therefore well-suited to applications such as high-speed caches and video memories. A read access time of 3.8 ns at a power dissipation of 520 mW has been achieved in an experimental 4K multiplied by 1-bit two-port memory integrated in a 1.5- mu m 5-GHz BiCMOS technology. The access time in this prototype design is nearly temperature-insensitive, increasing to only 4 ns at a case temperature of 100 degree C. 13 Refs.

34/3,AB/19 (Item 13 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02723208
E.I. Monthly No: EI8903020925
Title: 16 ns 256k multiplied by 1 CMOS SRAM.
Author: Flannagan, Stephen; Nogle, Scott; Faber, Allen; Herr, Norm; Mauntel, Rick; Engles, Bruce; Kung, Roger
Corporate Source: Motorola Memory Products Div, Austin, TX, USA
Conference Title: 1988 IEEE International Solid-State Circuits Conference - Digest of Technical Papers (31st ISSCC). First Edition.
Conference Location: San Francisco, CA, USA Conference Date: 19880217
E.I. Conference No.: 11868
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference. Publ by Lewis Winner, Coral Gables, FL, USA.. Available from IEEE Service Cent (cat n 88CH2562-7) Piscataway, NJ, USA. p 182-183, 360
Publication Year: 1988
CODEN: DTPCDE
Language: English
Abstract: A 256K multiplied by 1 SRAM (static **random-access**

memory) fabricated with a double-metal 1.2- mu m CMOS process is reported. Duplicated pads allow for multiple-package compatibility. The chip architecture uses sixteen subarray blocks to reduce power consumption, and local **word-lines** and **bit-lines** to assist in signal development. The address buffer design uses dual input stages to overcome the traditional difficulty of providing uniform dc margins in the presence of hysteresis. The active current is shown as a function of V//D//D// and as a function of cycle time. At 5 V, the active current is 48 mA at a 40 ns cycle (25 MHz).

34/3,AB/20 (Item 14 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02720814
E.I. Monthly No: EI8903020915
Title: 4 nsec 4K multiplied by 1 bit two-port BiCMOS SRAM.
Author: Yang, T. S.; Horowitz, M. A.; Wooley, B. A.
Corporate Source: Stanford Univ, CA, USA
Conference Title: Proceedings of the IEEE 1988 Custom Integrated Circuits Conference.
Conference Location: Rochester, NY, USA Conference Date: 19880516
E.I. Conference No.: 11798
Source: Proceedings of the Custom Integrated Circuits Conference. Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (cat n 88CH2584-1) Piscataway, NJ, USA. p 4.7/1-4
Publication Year: 1988
CODEN: PCICER
Language: English
Abstract: The authors introduce a two-port BiCMOS (bipolar complementary metal-oxide semiconductor) static memory cell that combines ECL (emitter-coupled-logic)-level **word-line** voltage swings and emitter-follower **bit line** coupling with a static CMOS latch to achieve access times comparable to those of high-speed bipolar SRAMs (static **random-access memories**), while preserving the high density and low power of CMOS memory arrays. The memory can be accessed for read and write independently and simultaneously, making it especially attractive for the design of video, cache, and other application-specific memories. An experimental 4K multiplied by 1 bit two-port memory integrated in a 1.5- mu m-5-GHz BiCMOS technology exhibits a read access time of 4 ns and a power dissipation of 550 mW. 4 Refs.

34/3,AB/21 (Item 15 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02518771
E.I. Monthly No: EI8802012209
Title: 25-NS 1-MBIT CMOS SRAM WITH LOADING-FREE **BIT LINES**.
Author: Matsui, Masataka; Ohtani, Takayuki; Tsujimoto, Jun-ichi; Iwai, Hiroshi; Suzuki, Azuma; Sato, Katsuhiko; Isobe, Mitsuo; Hashimoto, Kazuhiko ; Saitoh, Mitsuchika; Shibata, Hideki; Sasaki, Hisayo; Matsuno, Tadashi; Matsunaga, Jun-ichi; Iizuka, Tetsuya
Corporate Source: Toshiba Corp, Kawasaki, Jpn
Source: IEEE Journal of Solid-State Circuits v SC-22 n 5 Oct 1987 p 733-740
Publication Year: 1987
CODEN: IJSCBC ISSN: 0018-9200
Language: ENGLISH

Abstract: A 128K X 8-b CMOS SRAM is described which achieves a 25 ns access time, less than 40 mA active current at 10 MHz, and 2 MU A standby current. The novel **bit-line** circuitry (loading-free **bit line**), using two kinds of NMOSFETs with different threshold voltages, improves **bit-line** signal speed and integrity. The two-stage local amplification technique minimizes the data-line delay. The dynamic double-**word-line** scheme (DDWL) allows the cell array to be divided into 32 sections along the **word-line** direction without a huge increase in chip area. This allows the DDWL scheme to reduce the core-area delay time and operating power to about half that of other conventional structures. A double-metal 0. 8 MU m twin-tub CMOS technology has been developed to realize the 5. 6 X 9. 5 MU **2 cell size and the 6. 86 X 15. 37 mm**2 chip size. 10 refs.

34/3,AB/22 (Item 16 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02518758
E.I. Monthly No: EI8802012200
Title: 4-MBIT DRAM WITH FOLDED-**BIT-LINE** ADAPTIVE SIDEWALL-ISOLATED CAPACITOR (FASIC) CELL.
Author: Mashiko, Koichiro; Nagatomo, Masao; Arimoto, Kazutami; Matsuda, Yoshio; Furutani, Kiyohiro; Matsukawa, Takayuki; Yamada, Michihiro; Yoshihara, Tsutomu; Nakano, Takao
Corporate Source: Mitsubishi Electric Corp, Jpn
Source: IEEE Journal of Solid-State Circuits v SC-22 n 5 Oct 1987 p 643-650
Publication Year: 1987
CODEN: IJSCBC ISSN: 0018-9200
Language: ENGLISH
Abstract: A 5-V 4-Mb word X 1-b/1-Mb word X 4-b dynamic RAM with a static column mode and fast page mode has been built in a 0. 8 MU m twin-tub CMOS technology with single-metal, two-polycide, and single poly-Si interconnections. It uses an innovative folded-**bit-line** adaptive sidewall-isolated capacitor (FASIC) cell that measures 10. 9 MU m**2 and requires only a 2 MU m trench to obtain a storage capacitor of 50 fF with 10 nm SiO//2 equivalent dielectric film. A shared-**PMOS** sense-amplifier architecture used in this DRAM provides a low power consumption, small C//B-to-C//S capacitance ratio, and accurate reference level for the nonboosted **word-line** scheme with little area penalty. These concepts have allowed the DRAM to be housed in the industry standard 300 mil dual-in-line package with performances of 90 ns RAS access time and 30 ns column address access time. 21 refs.

34/3,AB/23 (Item 17 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02276801
E.I. Monthly No: EIM8710-065776
Title: 25NS 1 MB CMOS SRAM.
Author: Ohtani, Takayuki; Hashimoto, Kazuhiko; Matsui, Masataka; Tsujimoto, Jun-ichi; Iwai, Hiroshi; Saitoh, Mitsuchika; Shibata, Hideki; Sasaki, Hisayo; Isobe, Mitsuo; Matsunaga, Jun-ichi; Iizuka, Tetsuya
Corporate Source: Toshiba Corp, Kanagawa, Jpn
Conference Title: 1987 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, First Edition.
Conference Location: New York, NY, USA Conference Date: 19870225

E.I. Conference No.: 10107
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1987. Publ by Lewis Winner, Coral Gables, FL, USA. Available from IEEE Service Cent (Cat n 87CH2367-1), Piscataway, NJ, USA p 264-265, 420
Publication Year: 1987
CODEN: DTPCDE
Language: English
Abstract: Summary form only given. The development of a 1-Mb chip with a typical address access time of 25 ns and typical operating current of 15 mA is described. Desired performance has been realized by **bit-line** circuitry, a two-stage sense amplifier utilizing renewed double **word-line** structure, address transition detection techniques, and a 0. 8- MU m CMOS process with double-level polysilicon and double-level aluminum layers. 1 ref.

34/3,AB/24 (Item 18 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02276798
E.I. Monthly No: EIM8710-065773
Title: 35 NS 1 MB CMOS SRAM.
Author: Komatsu, Takaaki; Okazaki, Nobumichi; Nishihara, Toshiyuki; Kayama, Shigeki; Hoshi, Naoya; Aoyama, Jun-ichi; Shimada, Takashi
Corporate Source: Sony Corp, Kanagawa, Jpn
Conference Title: 1987 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, First Edition.
Conference Location: New York, NY, USA Conference Date: 19870225
E.I. Conference No.: 10107
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1987. Publ by Lewis Winner, Coral Gables, FL, USA. Available from IEEE Service Cent (Cat n 87CH2367-1), Piscataway, NJ, USA p 258-259, 417
Publication Year: 1987
CODEN: DTPCDE
Language: English
Abstract: The RAM described is usable at TTL I/O levels and exhibits improved noise immunity. The RAM utilizes a divided **word line** with a memory cell array divided into 16 sections. Each section includes 1024 PLUS 8 rows, or columns, 8 I/Os and 8 sense amplifiers. Only 8 pairs of short data lines are connected to one sense amplifier. This architecture expedites sensing of the information on the selected **bit lines**. A zero V//t//h **NMOS** is used to balance the **bit line** voltages. As a result, the equalizing period is reduced to half that of a conventional **PMOS** scheme in the write recovery mode. The RAM was fabricated with double-polysilicon, double-aluminum CMOS technology, using 1. 0- MU m design rules. The memory cell measures 6. 4- MU m X 11. 6- MU m. 3 refs.

34/3,AB/25 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08850785 Genuine Article#: 335ZH Number of References: 15
Title: Plasma enhanced chemical vapor deposition Si-rich silicon oxynitride films for advanced self-aligned contact oxide etching in sub-0.25 mu m ultralarge scale integration technology and beyond (ABSTRACT AVAILABLE)

Author(s): Kim JH (REPRINT) ; Yu JS; Ku JC; Ryu CK; Oh SJ; Kim SB; Kim JW; Hwang JM; Lee SY; Kouichiro I
Corporate Source: HYUNDAI ELECT IND CO LTD,SEMICOND ADV RES DIV, SAN 136-1/INCHON 467701/KYONGKI/SOUTH KOREA/ (REPRINT); TEL KOREA LTD,/YONGIN 449840/KYOUNGKI/SOUTH KOREA/; TOKYO ELECTRON YAMANASHI LTD,/YAMANASHI 407//JAPAN/
Journal: JOURNAL OF VACUUM SCIENCE & TECHNOLOGY A-VACUUM SURFACES AND FILMS , 2000, V18, N4,1 (JUL-AUG), P1401-1410
ISSN: 0734-2101 Publication date: 20000700
Publisher: AMER INST PHYSICS, 2 HUNTINGTON QUADRANGLE, STE 1NO1, MELVILLE, NY 11747-4501
Language: English Document Type: ARTICLE
Abstract: We intentionally introduced excessive Si during the SiOxNy film deposition in order to increase the etch selectivity-to-SiOxNy for advanced self-aligned contact (SAC) etching in sub-0.25 mu m ultralarge scale integration devices. The SiOxNy layer was deposited at a conventional plasma enhanced chemical vapor deposition chamber by using a mixture of SiH4, NH3, N2O, and He. The gas mixing ratio was optimized to get the best etch selectivity and low leakage current. The best result was obtained at 10% Si-SiOxNy. In order to employ SiOxNy film as an insulator as well as a SAC barrier, the leakage current of SiOxNy film was evaluated so that SiOxNy may have the low leakage current characteristics. The leakage current of 10% Si-SiOxNy film was 7 x 10(-9) A/cm(2). Besides, the Si-rich SiOxNy layer excellently played the roles of antireflection coating for **word line** and **bit line** photoresist patterning and sidewall spacer to build a **metal-oxide-semiconductor transistor** as well as a SAC oxide etch barrier. The contact oxide etching with the Si-rich SiOxNy film was done using C4F8/CH2F2/Ar in a dipole ring magnet plasma. As the C4F8 flow rate increases, the oxide etching selectivity-to-SiOxNy increases but etch stop tends to happen. Our optimized contact oxide etch process showed the high selectivity to SiOxNy larger than 25 and a wide process window (greater than or equal to 5 sccm) for the C4F8 flow rate. When the Si-rich SiOxNy SAC process was applied to a gigabit **dynamic random access memory** of cell array, there was no electrical short failure between conductive layers. (C) 2000 American Vacuum Society. [S0734-2101(00) 16504-2].

34/3,AB/26 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

14481979 PASCAL No.: 00-0143646
Innovating SRAM design and test program for fast process related defect recognition and failure analysis
In-line methods and monitors for process and yield improvement : Santa Clara CA, 22-23 September 1999
COPPENS P; VANHOREBEEK G; DE BACKER E; YUAN X J
AJURIA Sergio, ed; JAKUBCZAK Jerome F, ed
Alcatel Microelectronics, Oudenaarde, Belgium; IMEC, Leuven, Belgium
International Society for Optical Engineering, Bellingham WA, United States.
In-line methods and monitors for process and yield improvement. Conference (Santa Clara CA USA) 1999-09-22
Journal: SPIE proceedings series, 1999, 3884 290-297
Language: English
A special SRAM has been designed as a yield enhancement vehicle in a 0.35 mu m CMOS technology. Extra design rules were added to encourage process defects on certain places and discourage them on others. From the failure

signature of a memory cell (0 or I failure) and its failure extent (single cell, double cell, **bitline**, **wordline** ,) one can uniquely determine the process related cause of the failure. A dedicated test program has been developed to find the most common failures in a memory cell (e.g. floating **bitline**, **bitline** shorted to ground or Vdd, shorts between the nodes of the cell,). The innovating characteristics of the design allow to link these failures in an SRAM with high probability to a process related defect and its location within the memory cell. By simply testing the SRAM the main cause of failure can be found which can help to drive yield improvement, without doing intensive failure analysis. In this paper the design philosophy and the test methodology of this SRAM are described, illustrated with some examples of process related defects that proved the usefulness and the strength of the design and the test program.

34/3,AB/27 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

11554885 PASCAL No.: 94-0437802
Superconductor-semiconductor memories
III. Electronics
GHOSHAL U; KROGER H; VAN DUZER T
GREEN Michael A, ed
Univ. California, electronics res. lab., dep. electrical eng. computer sci., Berkeley CA 94720, USA
Lawrence Berkeley Laboratory, Berkeley CA 94720, USA
Applied Superconductivity Conference, Terra incognita.
ASC'92. Conference (Chicago IL USA) 1992-08-23
Journal: IEEE Transactions on applied superconductivity, 1993, 3 (1 p.4) 2315-2318
Language: English
We describe new types of hybrid superconductor-semiconductor RAMs which utilize the current switches in superconductive electronics to remove important constraints on the design of semiconductor memories and achieve performances unattainable by the individual technologies separately. We focus on a voltage **word line** RAM architecture and illustrate the basic designs in terms of a low-T SUB c Josephson-CMOS technology which we are currently developing at UC Berkeley SUP 1 . We discuss the design of interface circuits, **word-line** drivers, memory cells, and fluxoelectronic current sensing of **bit lines** . Current projections for 4 K operation indicate that sub-nanosecond 64 kb RAMs using a 0.8 mu m CMOS technology

34/3,AB/28 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

11403025 PASCAL No.: 94-0233409
A 5.8-ns 256-kb BiCMOS TTL SRAM with T-shaped **bit line** architecture
SHIOMI T; WADA T; OHBAYASHI S; OHBA A; HONDA H; ISHIGAKI Y; HINE S; ANAMI K; SUZUKI K; SUMI T
Mitsubishi Electric Corp., Itami, Japan
Journal: IEEE journal of solid-state circuits, 1993, 28 (12) 1362-1369
Language: English
This paper presents a new **bit line** architecture named T-shaped **bit line** architecture (TSBA), which is suitable for

high speed, high density, and/or large bit-wide configuration SRAM's. TSBA, utilizing orthogonal complimentary **bit lines** in parallel with the **word lines**, is the solution to **bit line** pitch constraint for direct bipolar column sensing. This TSBA is applied to a 256-Kb SRAM with a typical access time of 5.8 ns. To achieve access times below 6 ns, this SRAM employs a bipolar Darlington column sense amplifier, a hierarchical column decoding scheme, a data bus shielding layout combined with TSBA, and a 0.8- mu m BiCMOS technology

34/3,AB/29 (Item 4 from file: 144)
DIALOG(R)File 144:Pascal

10637896 PASCAL No.: 93-0147174
A 15-ns 16-Mb CMOS SRAM with interdigitated **bit-line** architecture : Memory and logic
MATSUMIYA M; KAWASHIMA S; SAKATA M; OOKURA M; MIYABO T; KOGA T; ITABASHI K; MIZUTANI K; SHIMADA H; SUZUKI N
Fujitsu Ltd, Nakahara-ku Kawasaki 211, Japan
Journal: IEEE journal of solid-state circuits, 1992, 27 (11) 1497-1503
Language: English
This paper describes circuit techniques for a reduced-voltage-amplitude data bus, fast access 16-Mb CMOS SRAM. An interdigitated **bit-line** architecture reduces data bus line length, thus minimizing bus capacitance. A hierarchical sense amplifier consists of 32 local sense amplifiers and a current sense amplifier. The current sense amplifier is used to reduce the data bus voltage amplitude and the sensing of the 16-b data bus signals in parallel. With these techniques we achieved a fast access time of 15 ns and a small active power of 165 mW in a 16-Mb CMOS SRAM. A split-**word-line** layout memory cell, with double-gate **pMOS** thin-film transistors (TFT's), keeps the transistor width stable while providing high-stability memory cell characteristics

34/3,AB/30 (Item 5 from file: 144)
DIALOG(R)File 144:Pascal

10126303 PASCAL No.: 92-0332056
A 1-V operating 256-kb full-CMOS SRAM
SEKIYAMA A; SEKI T; NAGAI S; IWASE A; SUZUKI N; HAYASAKA M
Fujitsu VLSI Ltd, MOS LSI design div., Kasugai 487, Japan
Journal: IEEE journal of solid-state circuits, 1992, 27 (5) 776-782
Language: English
A I-V operating 256-kb full-CMOS SRAM to be used in 1.5-V battery-based applications is presented. A reference **word line** and address transition detection (ATD) are used as timing control techniques to achieve adjustable timing of critical signals with a 1.5-V battery. The key circuit of the pulse sequence block is the ATD pulse generator circuit. We use a newly modified Schmitt trigger delay circuit. To reduce supply line noise in the chip, we needed to lower the peak of **bit-line** charge-up current. This was done by applying a divided **word-line** technique and a newly adopted staggered **bit-line** equalizing pulse technique

34/3,AB/31 (Item 6 from file: 144)
DIALOG(R)File 144:Pascal

10075345 , PASCAL No.: 92-0280849
A pulsed sensing scheme with a limited **bit-line** swing
SCHEUERLEIN R E; KATAYAMA Y; KIRIHATA T; SAKAUE Y; SATOH A; SUNAGA T; YOSHIKAWA T; KITAMURA K; DHONG S H
IBM Japan, IBM res. lab., Chiyoda-ku Tokyo 102, Japan
Journal: IEEE journal of solid-state circuits, 1992, 27 (4) 678-682
Language: English
This paper presents a pulsed sensing scheme with a limited **bit-line** swing designed for 4-Mb CMOS high-speed DRAM's (HSDRAM's) and beyond. It uses a standard CMOS cross-coupled sense amplifier and limites the swing by means of a pulsed sense clock. The signal loss that would occur if the **bitline** swing was not exactly limited to one threshold above the **word-line** 's low level is avoided by using a small reference voltage generator and trench decoupling capacitors. The new sensing scheme was successfully implemented on an experimental HSDRAM fabricated by using 0.7- mu m L SUB e SUB f SUB f CMOS technology, and thus a high-speed random access time of 15 ns and a low power dissipation of 144 mW were obtained for 512-kb array activation with a fast cycle time of 60 ns at 3.6 V

37/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7340656 INSPEC Abstract Number: B2002-09-2550N-012
Title: Nanotechnology goals and challenges for electronic applications
Author(s): Bohr, M.T.
Author Affiliation: Intel Corp., Hillsboro, OR, USA
Journal: IEEE Transactions on Nanotechnology vol.1, no.1 p.56-62
Publisher: IEEE,
Publication Date: March 2002 Country of Publication: USA
CODEN: ITNECU ISSN: 1536-125X
SICI: 1536-125X(200203)1:1L.56:NGCE;1-J
Material Identity Number: N761-2002-001
U.S. Copyright Clearance Center Code: 1536-125X/02/$17.00
Language: English
Abstract: Si **metal-oxide-semiconductor** field-effect **transistor** (**MOSFET**) scaling trends are presented along with a description of today's 0.13- mu m generation transistors. Some of the foreseen limits to future scaling include increased subthreshold leakage, increased gate oxide leakage, increased transistor parameter variability and **interconnect** density and performance. Basic device and circuit requirements for electronic logic and memory products are described. These requirements need to be kept in mind when evaluating nanotechnology options such as carbon nanotube field-effect transistors (FETs), nanowire FETs, single electron transistors and molecular devices as possible future replacements for Si **MOSFETs**.
Subfile: B

37/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6444491 INSPEC Abstract Number: B2000-02-2550F-004
Title: Effects of methyl silsesquioxane electron-beam curing on device characteristics of logic and four-transistor static **random-access memory**
Author(s): Chi-Fan Lin; I-Chung Tung; Ming-Shiann Feng
Author Affiliation: Dept. of Mater. Sci. & Eng., Nat. Chiao Tung Univ., Hsinchu, Taiwan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) vol.38, no.11 p.6253-7
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: Nov. 1999 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199911)38:11L.6253:EMSE;1-I
Material Identity Number: F221-1999-021
Language: English
Abstract: The as-spun methyl silsesquioxane (MSQ) film cured by an electron beam (e-beam) did not show water absorption after a five-day exposure to ambient air. MSQ was applied to the triple-level metal (TLM) Logic and double-level metal (DLM) four-transistor (4-T) static **random-access memory** (SRAM) as intermetal dielectric by means of the non-etchback process. When MSQ treatment conditions were properly controlled, the top layer of the as-spun films was cured by e-beam exposure while the bottom layer of the film was thermally cured for a short period of time. The as-cured MSQ offered good surface planarity. In addition, neither via poisoning, bowing nor cracking was observed. The

results showed that, by the application of the e-beam cured MSQ in the fabrication of **interconnect** structures, the cache time of DLM4-TSRAM could be improved to 10 ns compared with 11.5 ns for the SRAM fabricated using the conventional furnace cure spin-on-glass (SOG) process (400 degrees C annealing for one hour). E-beam exposure has little effect on n-channel metal-oxide semiconductor (**NMOS**) device characteristics, such as saturation current, threshold voltage and channel length. In contrast, e-beam exposure has a significant effect on p-channel **MOS** (**PMOS**) device characteristics, resulting in a shift of the threshold voltage as well as an increase in the channel length. It is notable that the e-beam exposure almost did not affect **NMOS** device characteristics in the 4-T SRAM, since the **polysilicon** load resistor could serve as a shield against electron bombardment. In such a case, the resistance of the **polysilicon** load resistor was significantly decreased.

Subfile: B

37/3,AB/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

5594747 INSPEC Abstract Number: B9707-1265-003

Title: Technology challenges for integration near and below 0.1 mu m

Author(s): Asai, S.; Wada, Y.

Author Affiliation: Adv. Res. Lab., Hitachi Ltd., Saitama, Japan

Journal: Proceedings of the IEEE vol.85, no.4 p.505-20

Publisher: IEEE,

Publication Date: April 1997 Country of Publication: USA

CODEN: IEEPAD ISSN: 0018-9219

SICI: 0018-9219(199704)85:4L.505:TCIN;1-L

Material Identity Number: P019-97004

U.S. Copyright Clearance Center Code: 0018-9219/97/$10.00

Language: English

Abstract: Technology challenges for **silicon** integrated circuits with a design rule of 0.1 mu m and below are addressed. We begin by reviewing the state-of-the-art CMOS technology at 0.25 mu m currently in development, covering a logic-oriented processes and **dynamic random access memory** (DRAM) processes. CMOS transistor structures are compared by introducing a figure of merit. We then examine scaling guidelines for 0.1 mu m which has started to deviate for optimized performance from the classical theory of constant-field scaling. This highlights the problem of nontrivial subthreshold current associated with the scaled-down CMOS with low threshold voltages. **Interconnect** issues are then considered to assess the performance of microprocessors in 0.1 mu m technology. 0.1 mu m technology will enable a microprocessor which runs at 1000 MHz with 500 million transistors. Challenges below 0.1 mu m are then addressed. New transistor and circuit possibilities such as **silicon** on insulator (SOI), dynamic-threshold (DT) **MOSFET**, and back-gate input **MOS** (BMOS) are discussed. Two problems below 0.1 mu m are highlighted. They are threshold voltage control and pattern printing. It is pointed out that the threshold voltage variations due to doping fluctuations is a limiting factor for scaling CMOS transistors for high performance. The problem with lithography below 0.1 mu m is the low throughput for a single probe. The use of massively parallel scanning probe assemblies working over the entire wafer is suggested to overcome the problem of low throughput.

Subfile: B

37/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

03336148 INSPEC Abstract Number: B89023621
Title: Evolution of the **MOS** transistor-from conception to VLSI
Author(s): Sah Chih-Tang
Author Affiliation: Dept. of Electr. & Comput. Eng., Illinois Univ., Urbana, IL, USA
Journal: Proceedings of the IEEE vol.76, no.10 p.1280-326
Publication Date: Oct. 1988 Country of Publication: USA
CODEN: IEEPAD ISSN: 0018-9219
U.S. Copyright Clearance Center Code: 0018-9219/88/1000-1280$01.00
Language: English
Abstract: Historical developments of the **metal-oxide-semiconductor** field-effect **transistor** (**MOSFET**) during the last 60 years are reviewed, from the 1928 patent disclosures of the field-effect conductivity modulation concept and the semiconductor triode structures proposed by Lilienfeld to the 1947 Shockley-originated efforts which led to the laboratory demonstration of the modern **silicon**. **MOSFET** in 1960. A survey is then made of the milestones of the past 30 years leading to the latest submicron **silicon** logic CMOS (complementary **MOS**) and BICMOS (bipolar-junction transistor CMOS combined) arrays and the three-dimensional and ferroelectric extensions of Dennard's one-transistor **dynamic random access memory** (DRAM) cell. The status of the submicron lithographic technologies is summarized. Future trends of memory cell density and logic gate speed are projected. Comparisons of the switching speed of the **silicon MOSFET** with that of **silicon** bipolar and GaAs field-effect transistors are reviewed. The use of high-temperature superconducting wires and GaAs-on-Si monolithic semiconductor optical clocks to break the **interconnect**-wiring delay barrier is discussed.
Subfile: B

37/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

02271649 INSPEC Abstract Number: B84035132
Title: International Electron Devices Meeting 1983. Technical Digest
Publisher: IEEE, New York, NY, USA
Publication Date: 1983 Country of Publication: USA 760 pp.
Conference Sponsor: IEEE
Conference Date: 5-7 Dec. 1983 Conference Location: Washington, DC, USA
Language: English
Abstract: The following topics are dealt with: isolation and dielectrics; bipolar and CMOS integrated circuits; power **MOS**; GaAs ICs; HEMTS and contacts; linear beam devices; CMOS VLSI device issues; hot carriers and interface phenomena; high-power devices; CAD tools; gyrotrons; optical sources; **random access memories**; **silicon** on insulating substrates; low-voltage monolithic devices; integrated power devices; III-V heterostructure photodetectors; solid-state imaging devices; micrometer and submicrometer CMOS; optoelectronic device needs; advanced **MOS** technologies; lithography and **interconnects**; nonvolatile memories; integrated sensors and sensing devices; superconducting and novel device technologies; and infrared detectors. 197 papers were presented, of which 184 are published in full in the present proceedings, and 12 in summary form only. Abstracts of individual papers can be found under the relevant classification codes in this or other issues.

01/22/2003

Subfile: B

37/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

02079456 INSPEC Abstract Number: B83039961, C83028675
Title: Signal processing unit
Author(s): Boswell, J.
Author Affiliation: AEG Telefunken, Ulm, West Germany
Journal: NTG-Fachberichte vol.82 p.49-51
Publication Date: 1983 Country of Publication: West Germany
CODEN: NTGFDK ISSN: 0341-0196
Conference Title: Grossintegration (Large Scale Integration)
Conference Date: 7-9 March 1983 Conference Location: Baden-Baden, West Germany
Language: German
Abstract: The architecture of the signal processing unit (SPU) comprises an ROM connected to a program bus, and an input-output bus connected to a data bus and register through a pipeline multiplier accumulator (PMAC) and a pipeline arithmetic logic unit (PALU), each associated with a **random access memory** (RAM1,2). The system pulse frequency is from 20 MHz. The PMAC is further detailed, and has a capability of 20 mega operations per second. There is also a block diagram for the PALU, showing **interconnections** between the register block (RBL), separator for bus (BS), register (REG), shifter (SH) and combination unit. The first and second RAMs have formats 64*16 and 32*32 bits, respectively. Further data are a 5-V power supply and 2.5 micron N-channel **silicon** gate **MOS** technology with about 50000 transistors.
Subfile: B C

37/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

00660144 INSPEC Abstract Number: B74026525
Title: LOCMOS, a new technology for complementary **MOS** circuits
Author(s): Brandt, B.B.M.; Steinmaier, W.; Strachan, A.J.
Author Affiliation: Philips Res. Labs., Nijmegen, Netherlands
Journal: Philips Technical Review vol.34, no.1 p.19-23
Publication Date: 1974 Country of Publication: Netherlands
CODEN: PTREAN ISSN: 0031-7926
Language: English
Abstract: Noteworthy features of this new LOCMOS technique are a special P-diffusion to produce a boron-concentration profile with a maximum below the **silicon** surface (to prevent parasitic N-channels from forming along the 'LOCOS oxide'), and the use of the LOCOS oxide and the **interconnection** pattern for the gates as masks for the formation of the sources and drains. The article gives three examples of circuits made by the LOCMOS technique: an inverter circuit with a delay time of 3 to 5 seconds, an 8-bit shift register occupying an area of 2.5 mm/sup 2/ and operating up to a frequency of 10 MHz, and a 256-bit static **random-access memory** with a surface area of 5 mm/sup 2/ and an access time of 100 to 200 ns.
Subfile: B

37/3,AB/8 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1519265 NTIS Accession Number: N90-20281/3
Product Assurance Technology for Procuring Reliable, Radiation-Hard, Custom LSI/VLSI Electronics
(Report, Oct. 1984 - Sep. 1986)
Buehler, M. G. ; Allen, R. A. ; Blaes, B. R. ; Hicks, K. A. ; Jennings, G. A.
Jet Propulsion Lab., Pasadena, CA.
Corp. Source Codes: 014828000; JJ574450
Sponsor: National Aeronautics and Space Administration, Washington, DC.
Report No.: NAS 1.26:185954; JPL-PUBL-89-1; NASA-CR-185954
Jan 89 236p
Languages: English
Journal Announcement: GRAI9019; STAR2813
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A11/MF A02
Advanced measurement methods using microelectronic test chips are described. These chips are intended to be used in acquiring the data needed to qualify Application Specific Integrated Circuits (ASIC's) for space use. Efforts were focused on developing the technology for obtaining custom IC's from CMOS/bulk **silicon** foundries. A series of test chips were developed: a parametric test strip, a fault chip, a set of reliability chips, and the CRRES (Combined Release and Radiation Effects Satellite) chip, a test circuit for monitoring space radiation effects. The technical accomplishments of the effort include: (1) development of a fault chip that contains a set of test structures used to evaluate the density of various process-induced defects; (2) development of new test structures and testing techniques for measuring gate-oxide capacitance, gate-overlap capacitance, and propagation delay; (3) development of a set of reliability chips that are used to evaluate failure mechanisms in CMOS/bulk: **interconnect** and contact electromigration and time-dependent dielectric breakdown; (4) development of **MOSFET** parameter extraction procedures for evaluating subthreshold characteristics; (5) evaluation of test chips and test strips on the second CRRES wafer run; (6) two dedicated fabrication runs for the CRRES chip flight parts; and (7) publication of two papers: one on the split-cross bridge resistor and another on asymmetrical SRAM (static **random access memory**) cells for single-event upset analysis.

37/3,AB/9 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

1510654 NTIS Accession Number: PB90-203720
1-Mbit CMOS Static RAM, TC551001P
Kosakai, M. ; Shibata, H. ; Matsui, M.
Toshiba Corp., Tokyo (Japan).
Corp. Source Codes: 021559000
c1989 5p
Languages: Japanese
Journal Announcement: GRAI9016
Text in Japanese.
Included in Toshiba Review, v44 n12 p940-943 1989.
NTIS Prices: (Order as PB90-203704, PC A06/MF A01)
A 1-Mbit static RAM, with advanced 0.8-micro m VLSI technologies, has been developed. This RAM, utilizing highly-reliable LDD (lightly doped

drain) **MOSFET**'s with **polysilicon** side-wall spacer, self-aligned contact and multi-level metal **interconnects**, integrates 6.3-million elements on a 6.52-mm x 15.13-mm chip. With regard to the circuit design, a double word-line structure, a two-stage local sense-amplifier scheme and an automatic power-down function in both read and write cycles have been developed to provide high-speed and low-power operation. The new RAM offers an access time of 85ns, a power consumption of 35mW at 1MHz, and a typical standby power of 10 micro W.

37/3,AB/10 (Item 3 from file: 6)
DIALOG(R)File 6:NTIS

0417576 NTIS Accession Number: AD-771 063/5/XAB
Liquid Crystal Display Panel
(Quarterly technical rept. no. 3, 1 Dec 72-28 Feb 73)
Kmetz, A. R.
Texas Instruments Inc Dallas Central Research Labs
Corp. Source Codes: 403833
Report No.: TI-08-73-25; ECOM-0158-72-3
Nov 73 23p
Journal Announcement: GRAI7404
See also report dated Jul 73, AD-763 927.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
The objective of this program is to demonstrate the feasibility of developing an effective x-y addressed liquid crystal display by fabricating a three-inch square flat dynamic scattering device incorporating all addressing and drive circuitry for the display of alphanumeric and vector-graphical information at a resolution of 30 lines per inch. The reflective display will be built directly on a **silicon** substrate containing an **MOS random access memory** with interface drivers. To eliminate chip-to-chip **interconnections** inside the display, the substrate will be a mosaic of four 1.7-inch square integrated circuit chips with exceptionally low circuit density. A partial redesign of the **MOS** circuit layout to facilitate photomask generation for these very large devices by reticle composition has been completed. A mechanical prototype display was built. (Modified author abstract)

37/3,AB/11 (Item 4 from file: 6)
DIALOG(R)File 6:NTIS

0369098 NTIS Accession Number: N73-13732/XAB
Design, Processing, and Testing of LSI Arrays for Space Station
Lile, W. R. ; Hollingsworth, R. J.
Radio Corp. of America, Princeton, N.J.
Report No.: NASA-CR-123943; PRRL-72-CR-44
Oct 72 35p
Journal Announcement: GRAI7307; STAR1104
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A03/MF A01
The design of a **MOS** 256-bit **Random Access Memory**

(RAM) is discussed. Technological achievements comprise computer simulations that accurately predict performance; aluminum-gate COS/**MOS** devices including a 256-bit RAM with current sensing; and a **silicon** -gate process that is being used in the construction of a 256-bit RAM with voltage sensing. The Si-gate process increases speed by reducing the overlap capacitance between gate and source-drain, thus reducing the crossover capacitance and allowing shorter **interconnections** . The design of a Si-gate RAM, which is pin-for-pin compatible with an RCA bulk **silicon** COS/**MOS** memory (type TA 5974), is discussed in full. The Integrated Circuit Tester (ICT) is limited to dc evaluation, but the diagnostics and data collecting are under computer control. The **Silicon**-on-Sapphire Memory Evaluator (SOS-ME, previously called SOS Memory Exerciser) measures power supply drain and performs a minimum number of tests to establish operation of the memory devices. The Macrodata MD-100 is a micropro-grammable tester which has capabilities of extensive testing at speeds up to 5 MHz. Beam-lead technology was successfully integrated with SOS technology to make a simple device with beam leads. This device and the scribing are discussed. (Author)

37/3,AB/12 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05448207
E.I. No: EIP99124954854
Title: 0.25 mu m 600MHz 1.5V SOI 64b ALPHA microprocessor
Author: Kim, Young Wug; Park, Sung Bae; Ko, Young Gun; Kim, Kwang Il; Kim, Il Kwon; Bae, Kum Jong; Lee, Kyung Wook; Yu, Jin Oh; Chung, Uin; Suh, Kwang Pyuk
Corporate Source: Samsung Electronics Corp, Kyungki-Do, S Korea
Conference Title: Proceedings of the 1999 46th IEEE International Solid-State Circuits Conference (ISSCC'99)
Conference Location: San Francisco, CA, USA Conference Date: 19990215-19990217
E.I. Conference No.: 55474
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1999. p 432-433
Publication Year: 1999
CODEN: DTPCDE ISSN: 0193-6530
Language: English
Abstract: **Silicon**-on-insulator (SOI) transistors along with copper inter-connections offer a breakthrough for the 21st century microprocessor technology for performance, power, and cost. In this study, a 0.25 mu m FD-SOI 4-Metal CMOS 74b Alpha Microprocessor was fabricated that contains 9.66 million transistors and measures 14.4 multiplied by 14.5mm**2 at 600MHz operating frequency under typical operating conditions with 1.5V power supply along 2.0V interface. 2 Refs.

37/3,AB/13 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05109162
E.I. No: EIP98084356297
Title: Proceedings of the 1998 Symposium on VLSI Technology
Author: Anon (Ed.)
Conference Title: Proceedings of the 1998 Symposium on VLSI Technology
Conference Location: Honolulu, HI, USA Conference Date:

19980609-19980611
E.I. Conference No.: 48879
Source: Digest of Technical Papers - Symposium on VLSI Technology 1998. IEEE, Piscataway, NJ, USA,98CH36216. 223p
Publication Year: 1998
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: The proceedings contains 86 papers from the 1998 Symposium on VLSI Technology. Topics discussed include: static RAM; DRAM; **MOSFET**; **silicon** on insulator technology; flash memory technology; advanced shallow junction technology; VLSI manufacturing; reliability technology; deep sub-micron patterning; hot carriers; silicide and gate technology; shallow trench isolation; and advanced gate dielectrics.

37/3,AB/14 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04970697
E.I. No: EIP98034104365
Title: Proceedings of the 1997 International Electron Devices Meeting
Author: Anon (Ed.)
Conference Title: Proceedings of the 1997 International Electron Devices Meeting
Conference Location: Washington, DC, USA Conference Date: 19971207-19971210
E.I. Conference No.: 48095
Source: Proceedings of the IEEE Hong Kong Electron Devices Meeting 1997. IEEE, Piscataway, NJ, USA,97CH36103. 944p
Publication Year: 1997
CODEN: 002525
Language: English
Abstract: The proceedings contains 216 papers from the 1997 IEEE International Electron Devices Meeting. Topics discussed include: embedded **dynamic random access memory** technology; complementary metal oxide semiconductor devices; device **interconnect** technology; quantum electronics; single electron devices; detectors; sensors; display devices; flash memory technology; lasers; light emitting diodes; **silicon** on insulator technology; thin film transistor technology; and microelectromechanical devices.

37/3,AB/15 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04827518
E.I. No: EIP97093834313
Title: Proceedings of the 1997 International Symposium on VLSI Technology, Systems, and Applications
Author: Anon (Ed.)
Conference Title: Proceedings of the 1997 International Symposium on VLSI Technology, Systems, and Applications
Conference Location: Taipei, China Conference Date: 19970603-19970605
E.I. Conference No.: 46985
Source: International Symposium on VLSI Technology, Systems, and Applications, Proceedings 1997. IEEE, Piscataway, NJ, USA. 369p
Publication Year: 1997
CODEN: 002207
Language: English

Abstract: The proceedings contains 79 papers from the 1997 International Symposium on Very Large Scale Integration Technology, Systems, and Applications. Topics discussed include: virtual wafer fabrication; **metal oxide semiconductor** field effect **transistors**; bipolar complementary **metal oxide semiconductor**; single superchip; nanoscale **silicon** technology; low-voltage low-power circuit design; digital converters; digital frequency synthesizers; nonvolatile memory; flash memory; microprocessor system; static **random access memory**; digital signal processors; programmable media and graphic processors; delayed synchronizers; and substrate triggering field oxide device.

37/3,AB/16 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04001543
E.I. No: EIP94122461034
Title: Proceedings of the 1994 Symposium on VLSI Technology
Author: Anon (Ed.)
Conference Title: Proceedings of the 1994 Symposium on VLSI Technology
Conference Location: Honolulu, HI, USA Conference Date: 19940607-19940609
E.I. Conference No.: 21361
Source: Digest of Technical Papers - Symposium on VLSI Technology 1994. IEEE, Piscataway, NJ, USA,94CH3433-0. 164p
Publication Year: 1994
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: The proceedings contains 77 papers on VLSI circuits. Topics discussed include microprocessor chips, **MOSFETs**, gates (transistors), VLSI circuits, nonvolatile storage, capacitors, ferroelectric devices, electrolysis, CMOS integrated circuits, lithography, **random access memories** and dielectric materials.

37/3,AB/17 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03366508
E.I. Monthly No: EIM9201-001508
Title: 23rd International Conference on Solid State Devices and Materials - SSDM '91.
Author: Anon (Ed.)
Conference Title: 23rd International Conference on Solid State Devices and Materials - SSDM '91
Conference Location: Yokohama, Jpn Conference Date: 19910827
E.I. Conference No.: 15633
Source: Conference on Solid State Devices and Materials 1991. Publ by Business Cent for Acad Soc Japan, Tokyo, Jpn. 770p
Publication Year: 1991
CODEN: EACMES
Language: English
Abstract: Proceedings incorporates 261 papers that are grouped into over 30 subjects. These deal with: hot carrier reliability, dielectric, advanced **silicon** processing, electron devices, optical devices, **interconnections**, **silicon** related materials, **silicon** -on-insulator technology, gigascale integration, new SiGe materials, surface engineering for semiconductor nanostructures, Optoelectronic

devices, growth technology, design and applications of superconductor devices and materials, device simulation, DRAM (digital **random access memories**, ultraclean wafer processing, science and technology on ultraclean wafer processing, giant microelectronics, **MOSFETs** and new devices as well as surface engineering.

37/3,AB/18 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02518772
E.I. Monthly No: EI8802012210
Title: 40-NS/100-PF LOW-POWER FULL-CMOS 256K (32K X 8) SRAM.
Author: Gubbels, Will C. H.; Hartgring, Cornelis D.; Salters, Roelof H. W.; Lammerts, Jos A. M.; Tooher, Michael J.; Hens, Patrick F. P. C.; Bastiaens, Joseph J. J.; Van Dijk, Jan M. F.; Sprokel, Marc A.
Corporate Source: Philips Research Lab, Eindhoven, Neth
Source: IEEE Journal of Solid-State Circuits v SC-22 n 5 Oct 1987 p 741-747
Publication Year: 1987
CODEN: IJSCBC ISSN: 0018-9200
Language: ENGLISH
Abstract: A fast and low-power full-CMOS 256K (32K X 8-b) static RAM is described. Typical access time is 40 ns with a 100-pF load. Power dissipation is 100 mW at 10 MHz and < 1 MU W in standby mode. The low standby power has been achieved by introducing a novel six-transistor, **polysilicon-interconnected**, double-cross-coupled cell. A novel output buffer design, a data-transition detection (DTD) circuit, and several other circuit techniques are introduced to obtain the speed and low active power dissipation. This chip is made in a 1. 3- MU m, twin-tub, single-poly, double-metal technology with a p epi on p** PLUS substrate. 4 refs.

37/3,AB/19 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02320860
E.I. Monthly No: EI8710099412
Title: TI FINDS A NEW WAY TO SHRINK SRAM CELLS.
Author: Lineback, J. Robert
Corporate Source: Electronics, New York, NY, USA
Source: Electronics v 60 n 15 Jul 23 1987 p 63-64
Publication Year: 1987
CODEN: ELECEH
Language: ENGLISH
Abstract: In an attempt to shrink the cell size of fast static **random-access memories** and quadruple their bit count, Memory-technology researchers at Texas Instruments Inc. in Dallas have produced what they believe is the industry's smallest six-transistor SRAM cell, only 104 MU m**2. They did it by introducing a tiny, scalable titanium nitride strap that cross-connects **polysilicon** gates and the n PLUS and p PLUS junctions of six-transistor storage cells in CMOS SRAMs. This novel self-aligning local **interconnection** scheme can save up to 25% of the chip area, because the size of the transistor drains can be reduced. The drains can be smaller because they don't have to accommodate the relatively large buried contacts traditionally used for cross-coupling in fast SRAM products. Also, reductions in source-drain junction areas lowered parasitic capacitance. As a result, TI's SRAM designers say they

were able to boost device speed by 15% compared with memories with full buried contacts.

37/3,AB/20 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02258539
E.I. Monthly No: EIM8707-044931
Title: FABRICATION TECHNOLOGIES FOR DUAL 4-KBIT STACKED SRAM.
Author: Yamazaki, K.; Yoneda, M.; Ogawa, S.; Ueda, M.; Akiyama, S.; Terui, Y.
Corporate Source: Matsushita Electric Industrial Co, Moriguchi, Jpn
Conference Title: International Electron Devices Meeting 1986: IEDM - Technical Digest. International Electron Devices Meeting 1986: IEDM - Technical Digest.
Conference Location: Los Angeles, CA, USA Conference Date: 19861207
E.I. Conference No.: 09693
Source: Technical Digest - International Electron Devices Meeting 1986. Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (Cat n 86CH2381-2), Piscataway, NJ, USA p 435-438
Publication Year: 1986
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: The process technologies for realizing a three-dimensional (3-D) LSI are reported. These emphasize high-quality laser recrystallization and thermally stable **interconnects**. A homogeneous recrystallization of the **silicon** island array was achieved all over a wafer by the dual laser beam recrystallization method (DLB), in which the 2-D energy distribution of the laser beam was precisely controlled. Thermally stable **interconnects** in the first layer were realized by W wiring and stoichiometry-controlled W/WSi/Si contact structure. By these key technologies, the 8-kb CMOS static RAM with two-active layers has been fabricated. 9 refs.

37/3,AB/21 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02117428
E.I. Monthly No: EIM8609-060230
Title: NEW HIGH DENSITY FULL CMOS SRAM CELL USING **POLYSILICON INTERCONNECTION** STRUCTURE.
Author: Masuoka, Fujio; Ochii, Kiyofumi; Masuda, Masami; Kobayashi, Kiyoshi; Kondo, Takeo
Corporate Source: Toshiba Corp, Kawasaki, Jpn
Conference Title: International Electron Devices Meeting 1985 - Technical Digest.
Conference Location: Washington, DC, USA Conference Date: 19851201
E.I. Conference No.: 08245
Source: Technical Digest - International Electron Devices Meeting 1985. Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (Cat n 85CH2252-5), Piscataway, NJ, USA p 280-283
Publication Year: 1985
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: A new **polysilicon interconnected** full CMOS SRAM cell, with only three metal lines and having reduced latchup susceptibility and small cell area, is described. **PMOS** and **NMOS** drain

terminals are **interconnected** through a double **polysilicon** layer, and the metal lines comprise two bit lines and a power supply line, which enables the substrate to be strapped to the supply voltage level without any additional substrate bias area in the memory cell array. Applying this new technique to a memory cell using 1. 2- MU m ground rules, the cell size, 9. 9 X 14. 3 MU m**2 , is about 75% that of the conventional full CMOS cell and is expected to realize 256 K bit full CMOS SRAM. 5 refs.

37/3,AB/22 (Item 11 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02089671
E.I. Monthly No: EIM8605-028023
Title: 1985 INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE, ISSCC '85.
Author: Hewlett, Frank W. Jr. (Ed.); Anderson, Allan H. (Ed.)
Corporate Source: Sandia Natl Lab, CMOS Memory & Microprocessor Div, Albuquerque, NM, USA
Conference Title: 1985 International Solid-State Circuits Conference, ISSCC '85.
Conference Location: New York, NY, USA Conference Date: 19850213
E.I. Conference No.: 07876
Source: IEEE Journal of Solid-State Circuits v SC-20 n 5 Oct 1985 p 892-1060
Publication Year: 1985
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: This issue contains 25 conference papers dealing with memory and logic circuits and various semiconductor technologies use in the fabrication of these devices. Considered are: 1-MBit **dynamic random access memories** (DRAM) with additional levels of inter- connect and reduced **interconnect** sheet sensitivity, based on CMOS and **NMOS** technologies; 256 K-Bit static **random access memories** (SRAM) with innovations in the circuit design and layout in order to improve their performance and reduce their power; content addressable 1-Mbit read only memory (ROM) with error correction circuitry; Electrically Erasable Programmable ROM (EEPROM) using bipolar processes and various **silicon** and non-**silicon** logic circuits, among them gate arrays, emitter coupled logic (ECL) and programmable array logic (PAL).

37/3,AB/23 (Item 12 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01794636
E.I. Monthly No: EI8509076557
E.I. Yearly No: EI85029715
Title: CMOS MEMORIES REPLACING n-**MOS** IN MEGABIT STORAGE CHIPS.
Author: Cole, Bernard Conrad
Source: Electron Week v 57 n 33 Nov 26 1984 p 53-61
Publication Year: 1984
CODEN: ELWEEB
Language: ENGLISH
Abstract: The replacement of n-**MOS random access memory** (RAM) and progammable read only memory (PROM) chips with CMOS chips is discussed. Other memory trends like replacement of **interconnections**, processing characterizing and segmentation are also considered, as well as second-order effects, increasing storage charge, use

of polycides, double-**silicon** process, and others.

37/3,AB/24 (Item 13 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01786790
E.I. Monthly No: EI8508071405
E.I. Yearly No: EI85100961
Title: ACTIVATION AND REDISTRIBUTION OF IMPLANTS IN POLYSI BY RTP.
Author: Chow, Robert; Powell, Ronald A.
Corporate Source: Varian Associates, Thin Film Technology Div, Palo Alto, CA, USA
Source: Semiconductor International v 8 n 5 May 1985 p 108-113
Publication Year: 1985
CODEN: SITLDD ISSN: 0163-3767
Language: ENGLISH
Abstract: Polycrystalline **silicon** (**polysilicon**) is employed for a variety of purposes in the fabrication of microelectronic devices, including emitters in bipolar transistors, high-value load resistors in static **random access memory** circuits, and **interconnect** lines and gate electrodes in **MOS** integrated circuits. The required doping can be accomplished with precise control by use of ion implantation. Following ion implantation, **polysilicon** films are subjected to various high-temperature cycles, and the effect of dopant redistribution must be considered. Over the last several years, rapid thermal processing (RTP) has been developed as an alternative to conventional furnace annealing, whereby high-temperature steps are carried out in times so short that minimal dopant redistribution occurs. 18 refs.

37/3,AB/25 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

09327035 Genuine Article#: 391JT Number of References: 22
Title: Process outlook for analog and RF applications (ABSTRACT AVAILABLE)
Author(s): Bruines JJP (REPRINT)
Corporate Source: Philips Semicond,Chief Technol Off,POB 30008/NL-65 HK Nijmegen//Netherlands/ (REPRINT); Philips Semicond,Chief Technol Off,NL-65 HK Nijmegen//Netherlands/
Journal: MICROELECTRONIC ENGINEERING, 2000, V54, N1-2 (DEC), P35-48
ISSN: 0167-9317 Publication date: 20001200
Publisher: ELSEVIER SCIENCE BV, PO BOX 211, 1000 AE AMSTERDAM, NETHERLANDS
Language: English Document Type: ARTICLE
Abstract: With every new CMOS technology node today, pure analogue design becomes more difficult, digital design more analogue, and RF design more feasible. Enabling new possibilities, such as RF-CMOS, while extending old ones is the challenge future technologies are facing.

Traditionally analog features, such as matching and cross-talk, are now entering the digital domain e.g. in Static **Random Access Memories** (SRAM) and clock tree design. Device and **interconnect** (compact) models must be able to cope with new technology steps like pocket implants and copper Damascene, while extending their capabilities for analogue and RF e.g. by modelling Non-QuasiStatic (NQS) effects. The System-on Chip (SoC) demand requires a multitude of high performance functionality's to be combined on one piece op **silicon**. It is obvious that this will lead to very complex processes. Finally, technology scaling, and the ever increasing

pressure on specifications, have triggered multi-die packages and **Silicon**-On-Anything (SoA).

37/3,AB/26 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02791242 Genuine Article#: MD639 Number of References: 9
Title: PERFORMANCE ANALYSIS OF MULTILAYER **INTERCONNECTIONS** FOR MEGABIT STATIC **RANDOM-ACCESS MEMORY** CHIP (Abstract Available)
Author(s): RAYAPATI VN; KAMINSKA B
Corporate Source: UNIV MONTREAL,ECOLE POLYTECH,DEPT ELECT ENGN/MONTREAL H3C 3J7/QUEBEC/CANADA/
Journal: IEEE TRANSACTIONS ON COMPONENTS HYBRIDS AND MANUFACTURING TECHNOLOGY, 1993, V16, N5 (AUG), P469-477
ISSN: 0148-6411
Language: ENGLISH Document Type: ARTICLE
Abstract: The objective of this paper is to analyze **interconnection** problems in the megabit static **random access memory** (SRAM) chip. A multilayer **interconnect** capacitance model is developed for the megabit SRAM chip. **Interconnection** effects on SRAM device performance parameters, such as propagation delay, speed, power consumption, and noise characteristics, are analyzed. A case study of 1-Mb SRAM chip **interconnection** problems is discussed. A multilayer **interconnect** approach is proposed for SRAM's to overcome on-chip **interconnection** difficulties. Implementing a double-layer **interconnect** approach, the wire length and chip size were reduced to 69% and 58% respectively. Maximum access time of 30.8 ns with 1 W at 100-degrees-C and wafer yield as high as 10% is achieved. Experimental results of multilayer **interconnections** for the 1-Mb SRAM are provided. The analysis results are found to be very useful for future megabit SRAM's.

37/3,AB/27 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04412237 JICST ACCESSION NUMBER: 00A0057129 FILE SEGMENT: JICST-E
Effects of Methyl Silsesquioxane Electron-Beam Curing on Device Characteristics of Logic and Four-Transistor Static **Random-Access Memory**.
LIN C-F (1); TUNG I-C (1); FENG M-S (1)
(1) National Chiao Tung Univ., Taiwan, Chn
Jpn J Appl Phys Part 1, 1999, VOL.38,NO.11, PAGE.6253-6257, FIG.7, TBL.4, REF.4
JOURNAL NUMBER: G0520BAE ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 539.2.09:539.12.04:621.315.592
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The as-spun methyl silsesquioxane(MSQ) film cured by an electron beam(e-beam) did not show water absorption after a five-day exposure to ambient air. MSQ was applied to the triple-level metal(TLM) Logic and double-level metal(DLM) four-transistor(4-T) static **random-access memory**(SRAM) as intermetal dielectric by means of the non-etchback process. When MSQ treatment conditions were properly controlled, the top layer of the as-spun films was cured by e-beam

exposure while the bottom layer of the film was thermally cured for a short period of time. The as-cured MSQ offered good surface planarity. In addition, neither via poisoning, bowing nor cracking was observed. The results showed that, by the application of the e-beam cured MSQ in the fabrication of **interconnect** structures, the cache time of DLM 4-T SRAM could be improved to 10ns compared with 11.5ns for the SRAM fabricated using the conventional furnace cure spin-on-glass(SOG) process (400.DEG.C. annealing for one hour). E-beam exposure has little effect on n-channel metal-oxide-semiconductor(**NMOS**) device characteristics, such as saturation current, threshold voltage and channel length. In contrast, e-beam exposure has a significant effect on p-channel **MOS**(**PMOS**) device characteristics, resulting in a shift of the threshold voltage as well as an increase in the channel length. It is notable that the e-beam exposure almost did not affect **NMOS** device characteristics in the 4-T SRAM, since the **polysilicon** load resistor could serve as a shield against electron bombardment. In such a case, the resistance of the **polysilicon** load resistor was significantly decreased. (author abst.)

37/3,AB/28 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03597616 JICST ACCESSION NUMBER: 98A0527357 FILE SEGMENT: JICST-E
A 0.7-.MU.m-Pitch Double Level Al **Interconnection** Technology for 1-Gbit DRAMs using SiO2 Mask Al Etching and Plasma Enhanced Chemical Vapor Deposition SiOF.
YOKOYAMA T (1); YAMADA Y (1); KISHIMOTO K (1); USAMI T (1); KAWAMOTO H (1); UENO K (1); GOMI H (1)
(1) NEC Corp., Kanagawa, JPN
Jpn J Appl Phys Part 1, 1998, VOL.37,NO.3B, PAGE.1140-1144, FIG.11, REF.9
JOURNAL NUMBER: G0520BAE ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 539.23:669 621.382.002.2
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A 0.7-.MU.m-pitch double level aluminum (Al) **interconnection** technology on a 1-.MU.m-high step is established for 1-Gbit **dynamic random access memories** (DRAMs). A SiO2 film which has a high resistance to Al etching was used as the mask layer. 0.35-.MU.m-width Al wirings were fabricated even on a 1-.MU.m-high step. 0.2-.MU.m-spaces (aspect ratio=2.5) between the taper shaped Al lines were filled, for the first time, by a plasma enhanced chemical vapor deposition (PECVD) fluorine doped **silicon** oxide (SiOF) film (.EPSILON.=3.9). The SiOF film capped with the PECVD SiO2 film has enough stability for the process integration. It was confirmed that these technologies can be applied to a double level Al **interconnection** using a 0.3-.MU.m-diameter tungsten (W) plug. (author abst.)

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Technology challenges for integration near and below 0.1 mm
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ABSTRACT: Technology challenges for **silicon** integrated circuits with a design rule of 0.1 mm and below will be addressed. We begin by reviewing the state-of-the-art CMOS technology at 0.25 mm currently in development, covering a logic-oriented processes and **dynamic random access memory** (DRAM) processes. CMOS transistor structures are compared by introducing a figure of merit. We will then examine scaling guidelines for 0.1 mm which has started to deviate for optimized performance from the classical theory of constant field scaling. This will highlight the problem of nontrivial subthreshold current associated with the scaled-down CMOS with low threshold voltages. **Interconnect** issues are then considered to assess the performance of microprocessors in 0.1 mm technology. It will be confirmed that 0.1 mm technology will enable a microprocessor which runs at 1000 MHz with 500 million transistors. Challenges below 0.1 mm will then be addressed. New transistor and circuit possibilities such as **silicon** on insulator (SOI), dynamic-threshold (DT) **MOSFET** and back-gate-input **MOS** (BMOS) are discussed. Two most problems to become formidable below 0.1 mm are highlighted. They are threshold voltage control and pattern printing. It is pointed out that the threshold voltage variations due to doping fluctuations is a limiting factor for scaling CMOS transistors for high performance. The problem with the lithography below 0.1 mm is the low throughput for a single probe. The use of massively parallel scanning probe assemblies working over the entire wafer is suggested to overcome the problem of low throughput. Copyright 1997, IEEE.

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Titanium nitride local **interconnect** technology for VLSI
TANG T E; CHE-CHIA WEI; HAKEN R A; HOLLOWAY T C; HITE L R; BLAKE T G W
Texas Instruments corp., Dallas TX 75265, USA
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